

# Compal Confidential

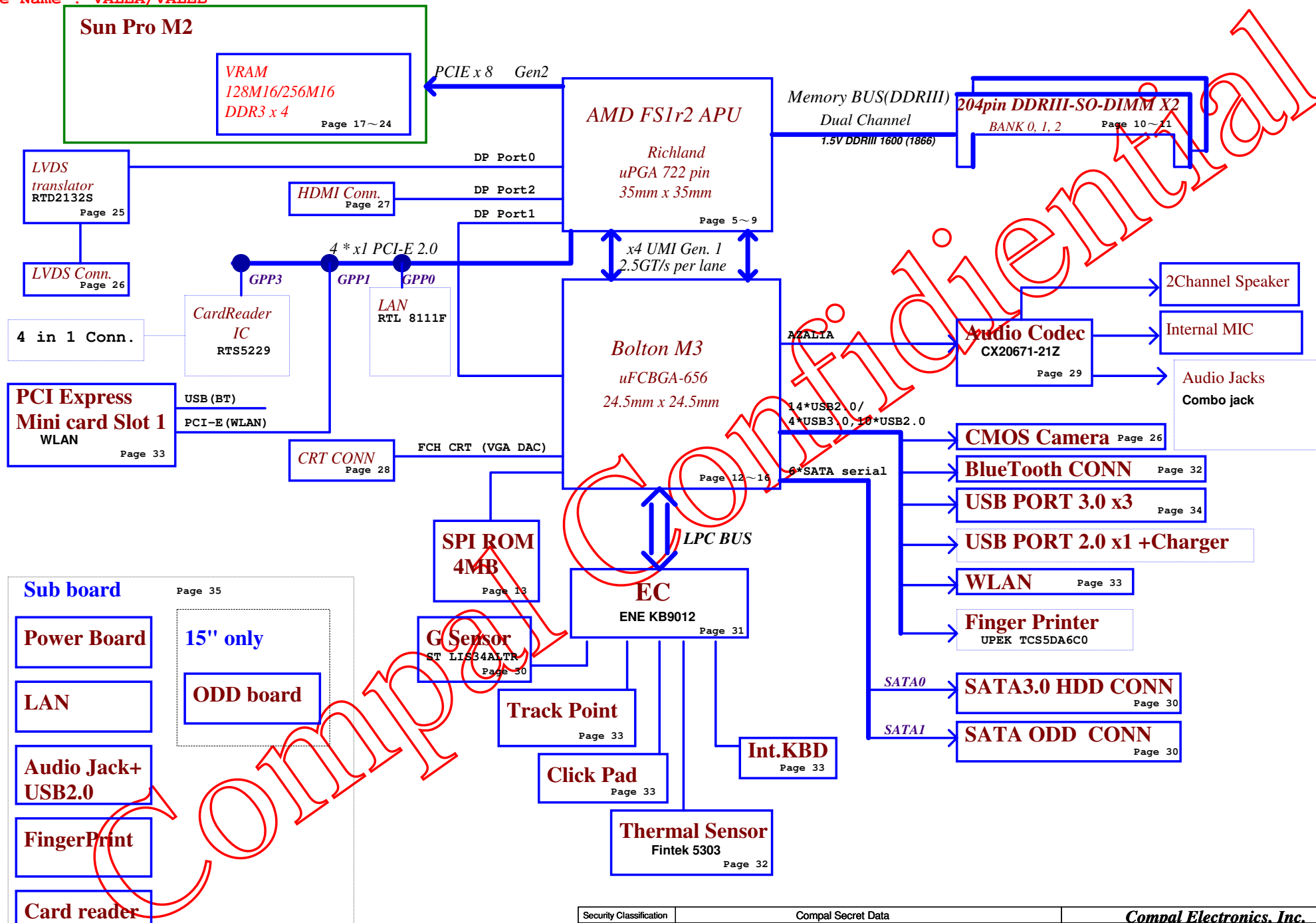
## VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Cover Page
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## Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Sun Pro M2	1000-0010b	82H
			LVDS translator		

## FCH SMB0

(FCH\_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

## Stencil Memo

## FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

## Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

## FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

## BOM Structure

UMA@ : UMA Only  
 DIS@ : DIS muxless  
 CMOS@ : USB camera  
 CONN@ : ME components  
 X76@, H1G@, S1G@ : VRAM

## BOM option and stencil

SDV:  
 CMOS@/DIS@ + X76@

PJ201, PJ401, PJ502, PJ503, PJ504, PJ601, PJ603, PJ604,  
 PJ701, PJ702, PJ703, PJ704, J1, J2301, J2401, J2402, J2403  
 PJ402, PJ403, PJ501, PJ602, PJ801, PJ802, PJ803, PJ805

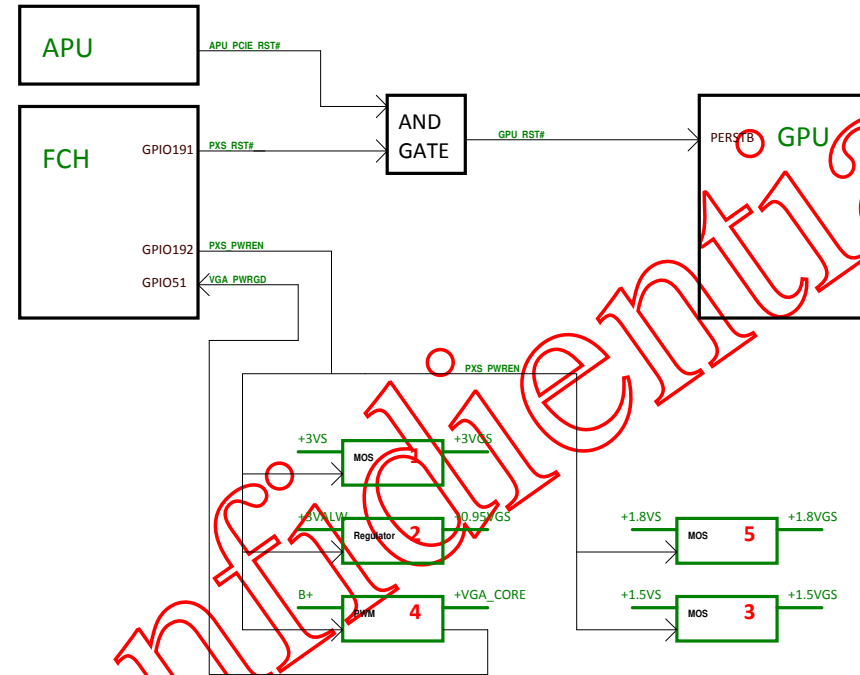
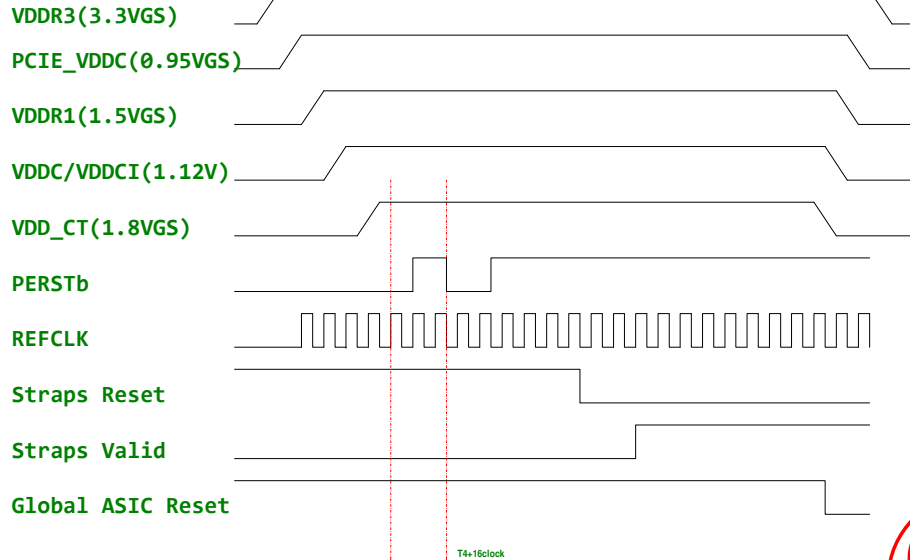
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Notes List

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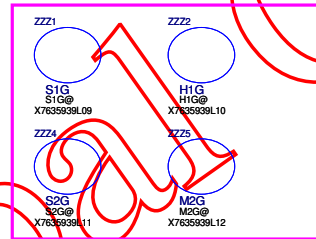
# Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



## SUN PRO VRAM STRAP

Vendor	PS 3[2]	PS 3[1]	PS 3[0]	R pu	R pd
H5TQ2G63DFR-11C SA00003Y070	0	0	0	R1430 NC	R1436 4.75K
K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
K4W4G1646B-BC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53K	R1436 4.99K
MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24K	R1436 5.62K
K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 3.24K	R1436 10k
	1	1	1	R1430 4.75K	R1436 NC



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[17] PCIE\_CRX\_GTX\_P[0..7]

[17] PCIE\_CRX\_GTX\_N[0..7]

PCIE\_CTX\_GRX\_P[0..7] [17]

PCIE\_CTX\_GRX\_N[0..7] [17]



JCPU1A

PCI EXPRESS

PCIE\_CRX\_GTX\_P0 AB8  
PCIE\_CRX\_GTX\_N0 AB7  
PCIE\_CRX\_GTX\_P1 AA9  
PCIE\_CRX\_GTX\_N1 AA8  
PCIE\_CRX\_GTX\_P2 AA5  
PCIE\_CRX\_GTX\_N2 AA6  
PCIE\_CRX\_GTX\_P3 Y8  
PCIE\_CRX\_GTX\_N3 Y7  
PCIE\_CRX\_GTX\_P4 W9  
PCIE\_CRX\_GTX\_N4 W8  
PCIE\_CRX\_GTX\_P5 W5  
PCIE\_CRX\_GTX\_N5 W6  
PCIE\_CRX\_GTX\_P6 V8  
PCIE\_CRX\_GTX\_N6 V7  
PCIE\_CRX\_GTX\_P7 U9  
PCIE\_CRX\_GTX\_N7 U8

P.GFX\_RXP0  
P.GFX\_RXN0  
P.GFX\_RXP1  
P.GFX\_RXN1  
P.GFX\_RXP2  
P.GFX\_RXN2  
P.GFX\_RXP3  
P.GFX\_RXN3  
P.GFX\_RXP4  
P.GFX\_RXN4  
P.GFX\_RXP5  
P.GFX\_RXN5  
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P.GFX\_RXN15

P.GFX\_TXP0  
P.GFX\_TXN0  
P.GFX\_TXP1  
P.GFX\_TXN1  
P.GFX\_TXP2  
P.GFX\_TXN2  
P.GFX\_TXP3  
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P.GFX\_TXP13  
P.GFX\_TXN13  
P.GFX\_TXP14  
P.GFX\_TXN14  
P.GFX\_TXP15  
P.GFX\_TXN15

AB2 PCIE\_CTX\_C\_GRX\_P0 C1 DIS@ 1  
AB1 PCIE\_CTX\_C\_GRX\_N0 C2 DIS@ 1  
AA3 PCIE\_CTX\_C\_GRX\_P1 C3 DIS@ 1  
AA2 PCIE\_CTX\_C\_GRX\_N1 C4 DIS@ 1  
Y5 PCIE\_CTX\_C\_GRX\_P2 C5 DIS@ 1  
Y4 PCIE\_CTX\_C\_GRX\_N2 C6 DIS@ 1  
W3 PCIE\_CTX\_C\_GRX\_P3 C7 DIS@ 1  
W2 PCIE\_CTX\_C\_GRX\_N3 C8 DIS@ 1  
W5 PCIE\_CTX\_C\_GRX\_P4 C9 DIS@ 1  
W4 PCIE\_CTX\_C\_GRX\_N4 C10 DIS@ 1  
V5 PCIE\_CTX\_C\_GRX\_P5 C11 DIS@ 1  
V4 PCIE\_CTX\_C\_GRX\_N5 C12 DIS@ 1  
V2 PCIE\_CTX\_C\_GRX\_P6 C13 DIS@ 1  
V1 PCIE\_CTX\_C\_GRX\_N6 C14 DIS@ 1  
U3 PCIE\_CTX\_C\_GRX\_P7 C15 DIS@ 1  
U2 PCIE\_CTX\_C\_GRX\_N7 C16 DIS@ 1

2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
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2 .1U 0402 16V7K  
2 .1U 0402 16V7K

PCIE\_CTX\_GRX\_P0  
PCIE\_CTX\_GRX\_N0  
PCIE\_CTX\_GRX\_P1  
PCIE\_CTX\_GRX\_N1  
PCIE\_CTX\_GRX\_P2  
PCIE\_CTX\_GRX\_N2  
PCIE\_CTX\_GRX\_P3  
PCIE\_CTX\_GRX\_N3  
PCIE\_CTX\_GRX\_P4  
PCIE\_CTX\_GRX\_N4  
PCIE\_CTX\_GRX\_P5  
PCIE\_CTX\_GRX\_N5  
PCIE\_CTX\_GRX\_P6  
PCIE\_CTX\_GRX\_N6  
PCIE\_CTX\_GRX\_P7  
PCIE\_CTX\_GRX\_N7

SDV/FVT, NO.1

SDV/FVT, NO.1

LAN

WLAN

[35] PCIE\_CRX\_DTX\_P0  
[35] PCIE\_CRX\_DTX\_N0  
[33] PCIE\_CRX\_DTX\_P1  
[33] PCIE\_CRX\_DTX\_N1

Card Reader

[35] PCIE\_CRX\_DTX\_P3  
[35] PCIE\_CRX\_DTX\_N3

[12] UMI\_RXP0  
[12] UMI\_RXN0  
[12] UMI\_RXP1  
[12] UMI\_RXN1  
[12] UMI\_RXP2  
[12] UMI\_RXN2  
[12] UMI\_RXP3  
[12] UMI\_RXN3

+1.2VS 1 R1 2 P\_ZVDDP 196\_0402\_1% AG11

AE5 P.GPP\_RXP0  
AE6 P.GPP\_RXN0  
AD8 P.GPP\_TXP1  
AD7 P.GPP\_TXN1  
AC9 P.GPP\_RXP2  
AC8 P.GPP\_RXN2  
AC5 P.GPP\_RXP3  
AC6 P.GPP\_RXN3

P.GPP\_TXP0  
P.GPP\_TXN0  
P.GPP\_TXP1  
P.GPP\_TXN1  
P.GPP\_TXP2  
P.GPP\_TXN2  
P.GPP\_TXP3  
P.GPP\_TXN3

AD5 PCIE\_CTX\_C\_DRX\_P0 C33 1  
AD4 PCIE\_CTX\_C\_DRX\_N0 C34 1  
AD2 PCIE\_CTX\_C\_DRX\_P1 C123 1  
AD1 PCIE\_CTX\_C\_DRX\_N1 C124 1

2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K

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PCIE\_CTX\_DRX\_N0 [35]  
PCIE\_CTX\_DRX\_P1 [33]  
PCIE\_CTX\_DRX\_N1 [33]

PCIE\_CTX\_DRX\_P3 [35]  
PCIE\_CTX\_DRX\_N3 [35]

AG8 P.UMI\_TXP0  
AG9 P.UMI\_TXN0  
AG6 P.UMI\_TXP1  
AG5 P.UMI\_TXN1  
AF7 P.UMI\_TXP2  
AF6 P.UMI\_TXN2  
AE8 P.UMI\_TXP3  
AE9 P.UMI\_TXN3

P.UMI\_TXP0  
P.UMI\_TXN0  
P.UMI\_TXP1  
P.UMI\_TXN1  
P.UMI\_TXP2  
P.UMI\_TXN2  
P.UMI\_TXP3  
P.UMI\_TXN3

AG2 UMI\_TXP0 C37 1  
AG3 UMI\_TXN0 C38 1  
AF4 UMI\_TXP1 C39 1  
AF5 UMI\_TXN1 C40 1  
AF1 UMI\_TXP2 C41 1  
AF2 UMI\_TXN2 C42 1  
AE2 UMI\_TXP3 C43 1  
AE3 UMI\_TXN3 C44 1

2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K  
2 .1U 0402 16V7K

UMI\_TXP0 [12]  
UMI\_TXN0 [12]  
UMI\_TXP1 [12]  
UMI\_TXN1 [12]  
UMI\_TXP2 [12]  
UMI\_TXN2 [12]  
UMI\_TXP3 [12]  
UMI\_TXN3 [12]

P\_ZVDDP

P\_ZVSS

LOTES\_ACA-ZIF-109-P12-A\_FST12  
CONN@

### Power Sequence of APU

+1.5V

+2.5VS

+1.5VS

+APU\_CORE

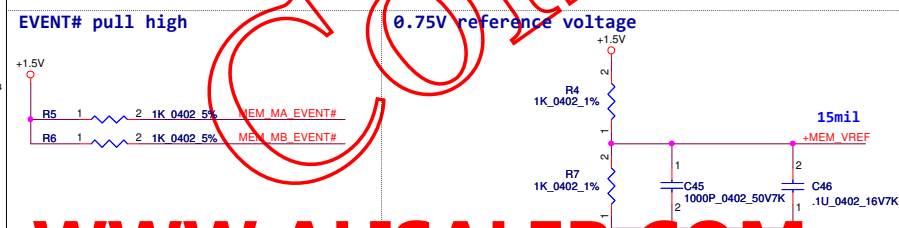
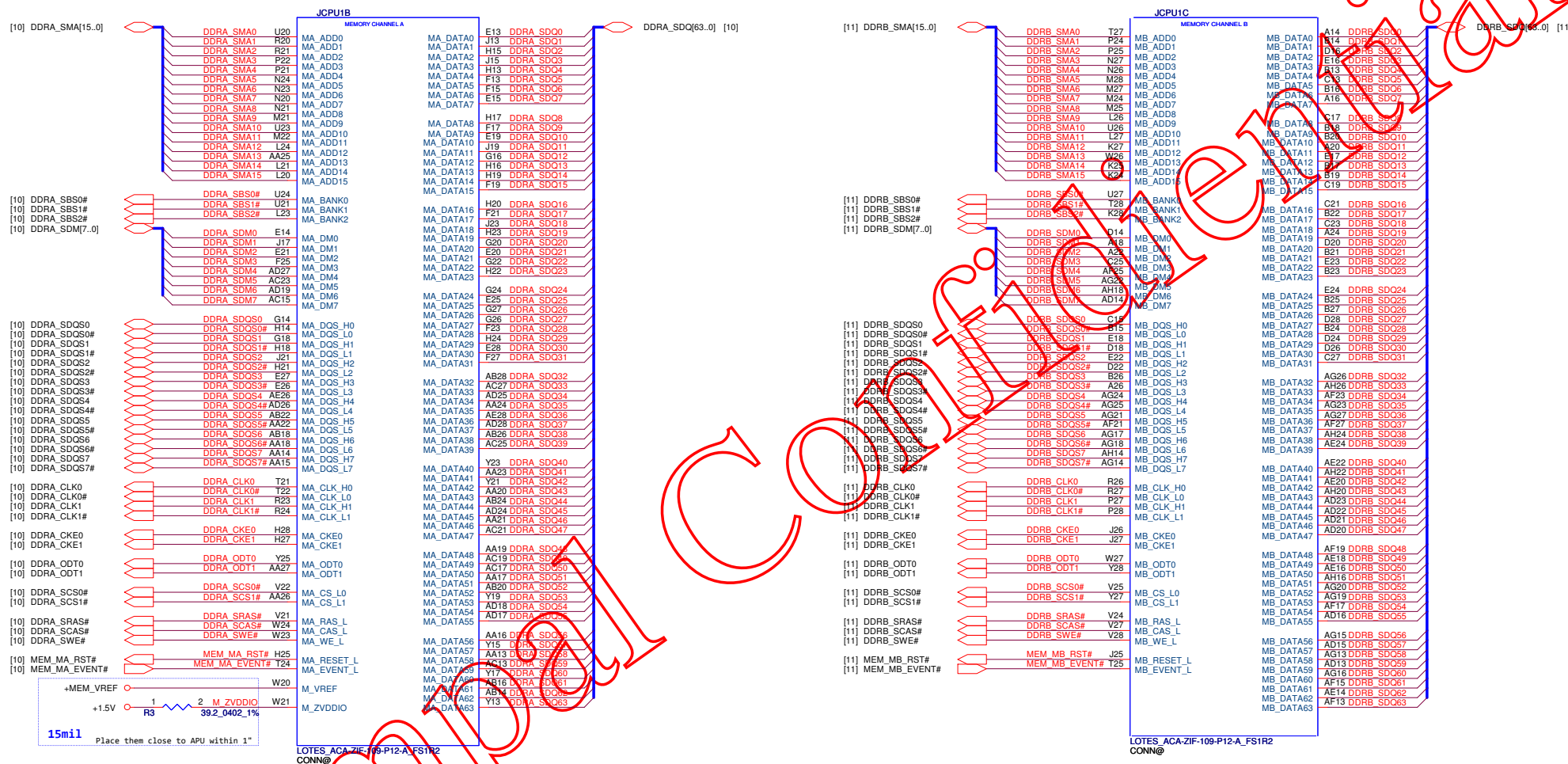
+APU\_CORE\_NB

+1.2VS

Group A

Group B

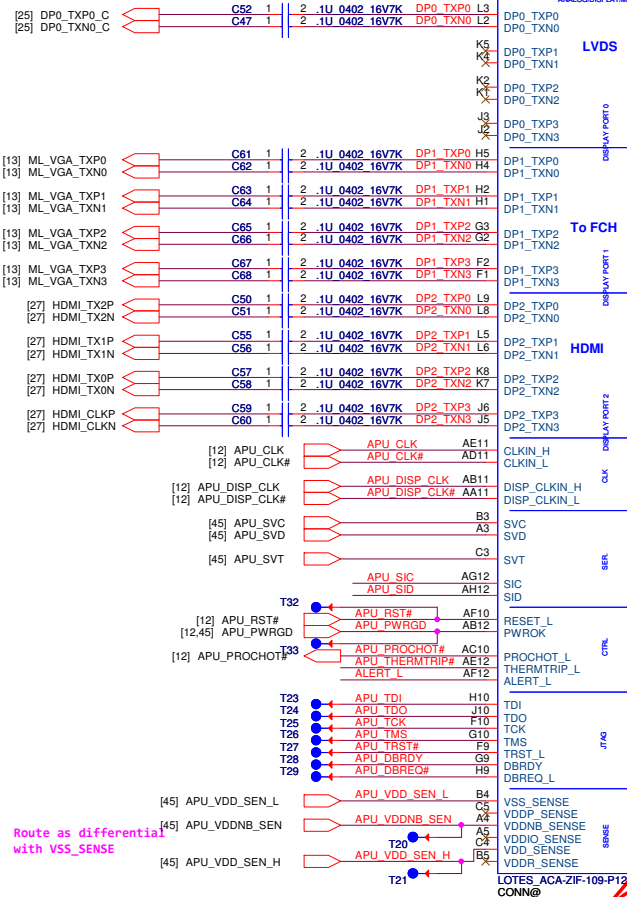
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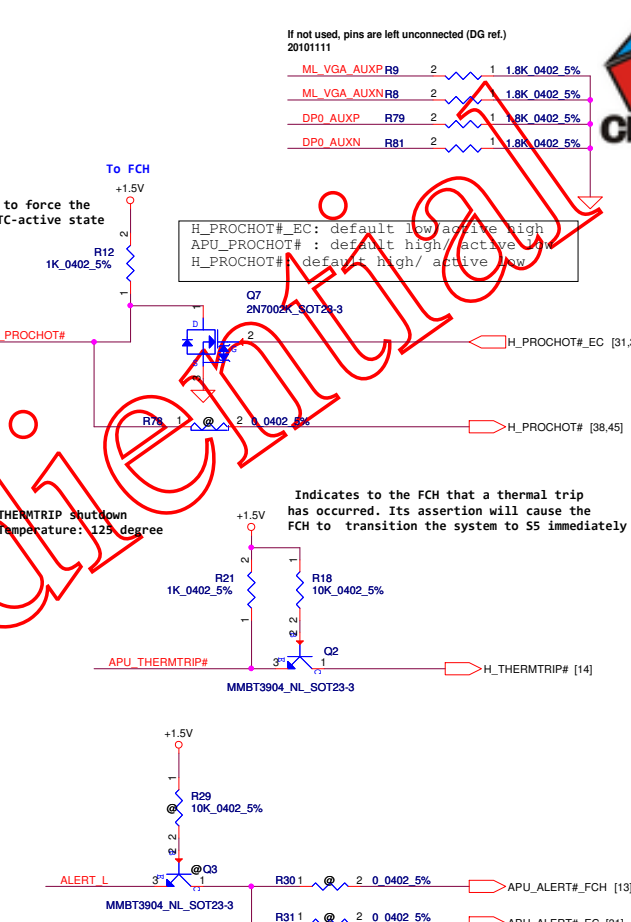
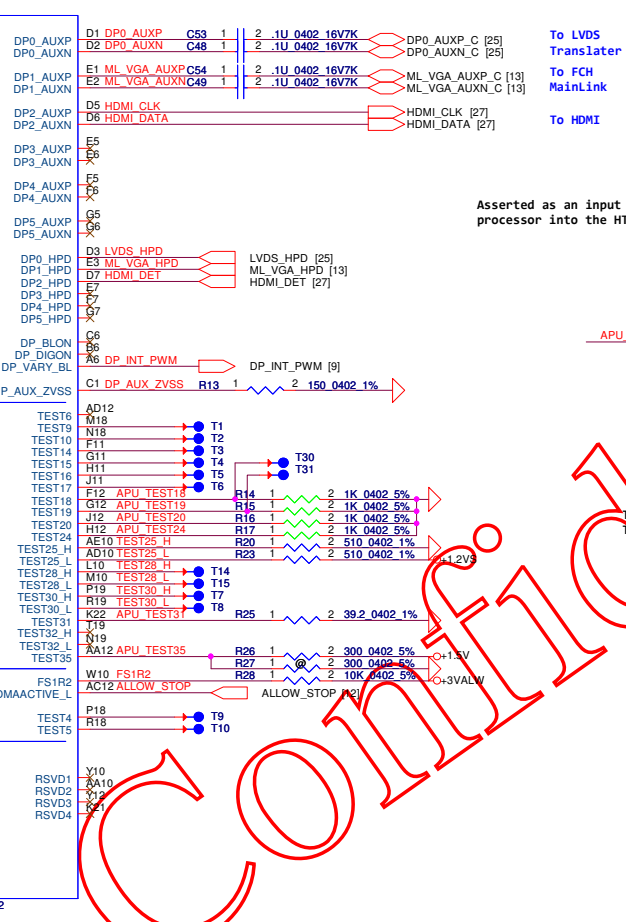
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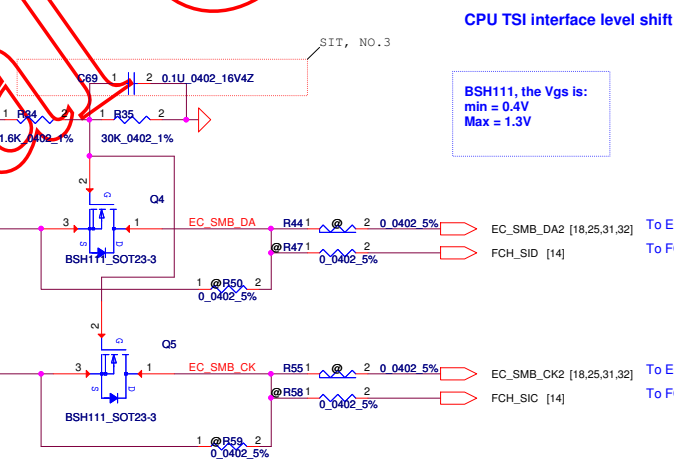
# Place near APU



# JCPU10D



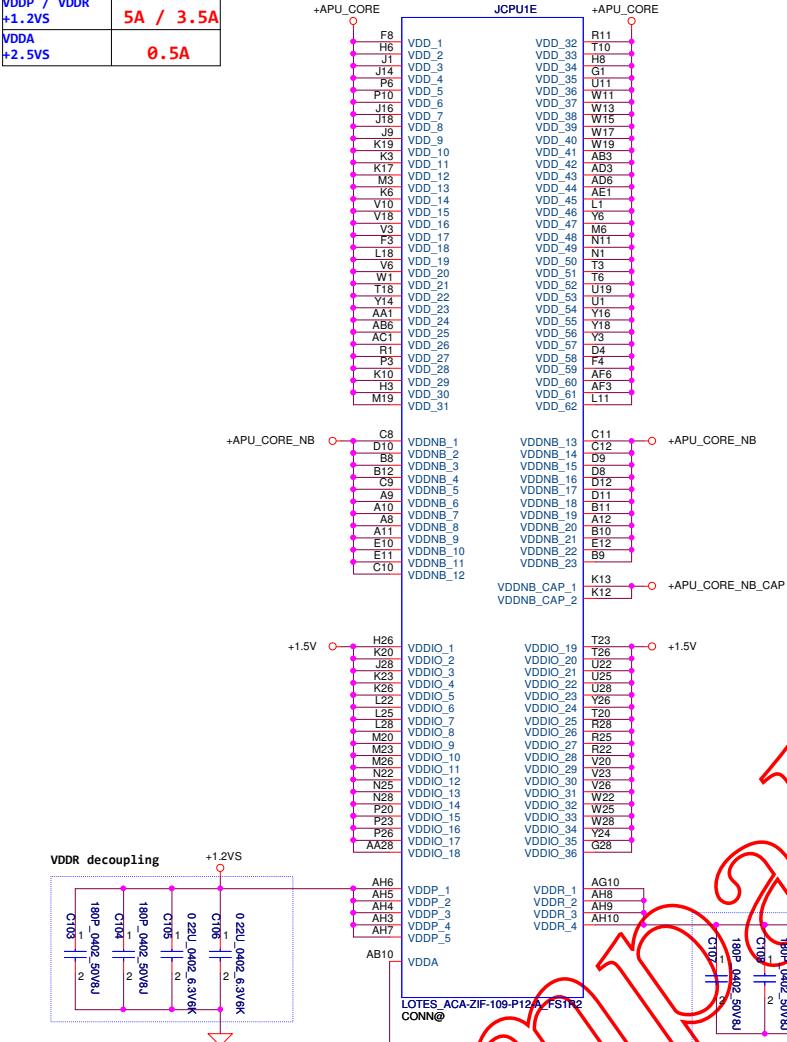
# CPU TSI interface level shift



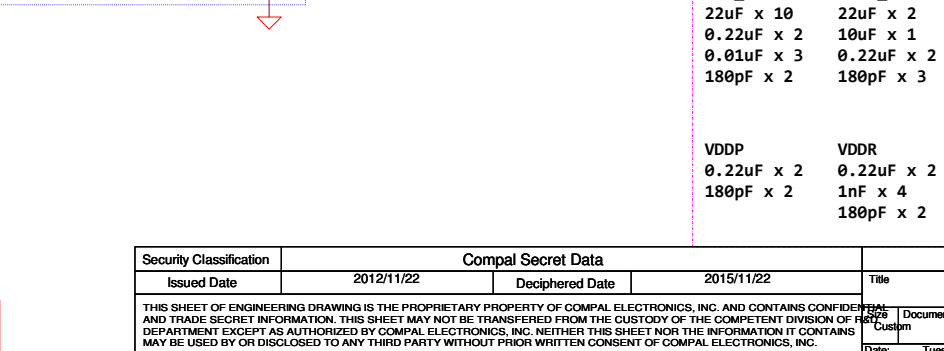
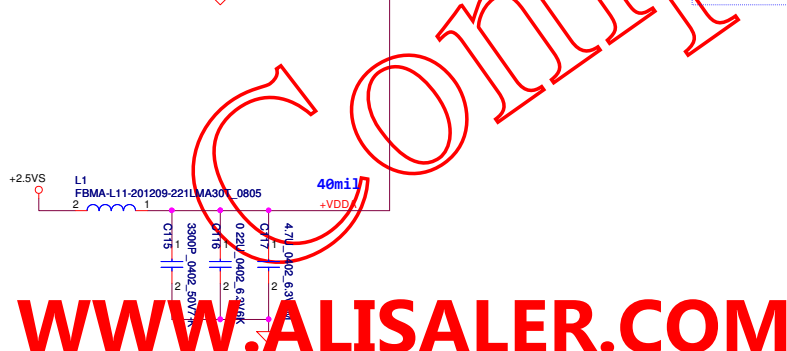
Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	ES1r2 Display/MISC/HDT	
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Power Name	Consumption
VDD	60A
+APU_CORE	
VDDNB	44A
+APU_CORE_NB	
VDDIO	3.2A
+1.5V	
VDDP / VDDR	5A / 3.5A
+1.2VS	
VDDA	
+2.5VS	0.5A



JCPU1E	
J20	VSS_1
L4	VSS_2
R7	VSS_3
W18	VSS_4
A15	VSS_5
AB17	VSS_6
AC22	VSS_7
AE21	VSS_8
AF24	VSS_9
AH23	VSS_10
AH25	VSS_11
B7	VSS_12
C14	VSS_13
C16	VSS_14
C2	VSS_15
C25	VSS_16
C28	VSS_17
D13	VSS_18
D15	VSS_19
D17	VSS_20
D27	VSS_21
E4	VSS_22
E9	VSS_23
F14	VSS_24
F16	VSS_25
F18	VSS_26
F20	VSS_27
F22	VSS_28
F28	VSS_29
G13	VSS_30
G17	VSS_31
G19	VSS_32
G21	VSS_33
G25	VSS_34
G4	VSS_35
G23	VSS_36
J24	VSS_37
J7	VSS_38
K14	VSS_39
K9	VSS_40
AC11	VSS_41
L19	VSS_42
L7	VSS_43
MT1	VSS_44
AF11	VSS_45
V19	VSS_46
V9	VSS_47
W16	VSS_48
W4	VSS_49
W7	VSS_50
Y11	VSS_51
Y20	VSS_52
Y22	VSS_53
Y9	VSS_54
A17	VSS_55
A13	VSS_56
K16	VSS_57
F24	VSS_58
G8	VSS_59
H7	VSS_60
J8	VSS_61
VSS_73	A21
VSS_74	A23
VSS_75	A25
VSS_76	A7
VSS_77	AA4
VSS_78	AB13
VSS_80	AB15
VSS_81	AB19
VSS_83	AB21
VSS_84	AB27
VSS_85	AB29
VSS_86	AB37
VSS_88	AC14
VSS_89	AC18
VSS_90	AC20
VSS_92	AC24
VSS_93	AC28
VSS_94	AC4
VSS_95	AC7
VSS_96	AD9
VSS_97	AE13
VSS_98	AE15
VSS_100	AE17
VSS_101	N10
VSS_102	N4
VSS_103	N7
VSS_104	Y10
VSS_105	R4
VSS_106	T11
VSS_108	T9
VSS_109	U7
VSS_110	U4
VSS_111	U7
VSS_112	V11
VSS_113	AE23
VSS_114	AE25
VSS_115	AE27
VSS_117	AE4
VSS_118	AE7
VSS_119	AF14
VSS_120	AF16
VSS_121	AF18
VSS_122	AF20
VSS_123	AF22
VSS_124	AF26
VSS_125	AF28
VSS_126	AF9
VSS_127	AG4
VSS_128	AG7
VSS_129	AH13
VSS_130	AH15
VSS_131	AH17
VSS_132	AH19
VSS_133	AH21
VSS_134	C18
VSS_135	C21
VSS_136	D21
VSS_137	W14
VSS_138	W18
VSS_139	C7
VSS_140	E8
VSS_141	K18
VSS_142	W12
VSS_143	

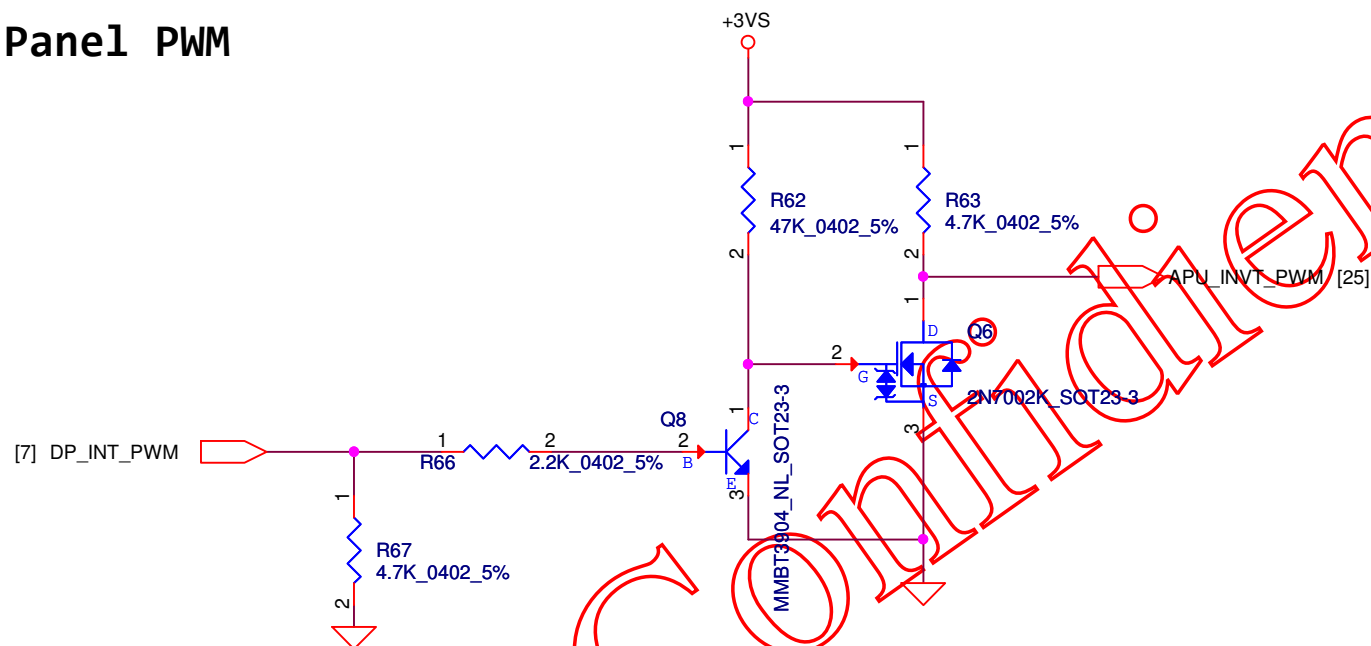


Demo Board Capacitor			
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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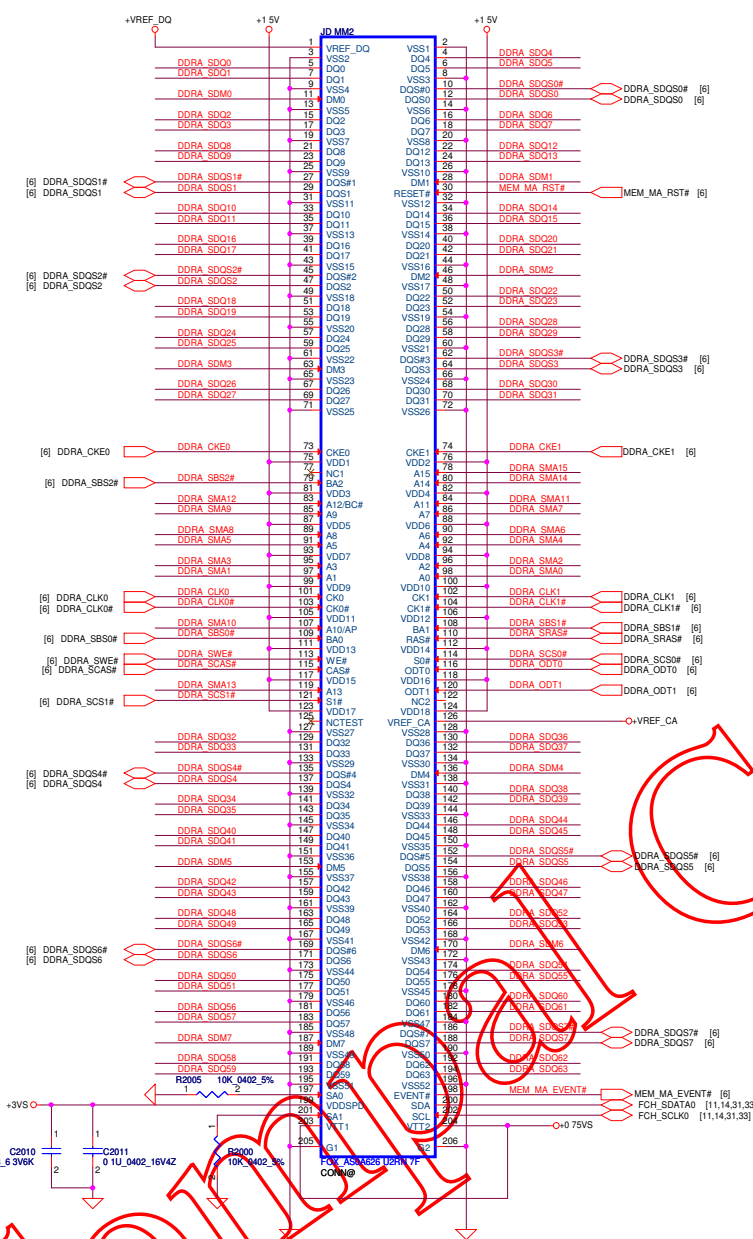
Security Classification	Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	FS1r2 PWR/GND
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# Panel PWM

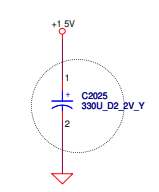
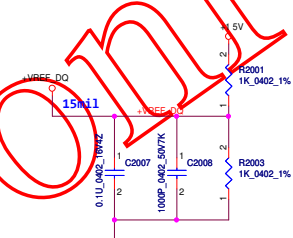
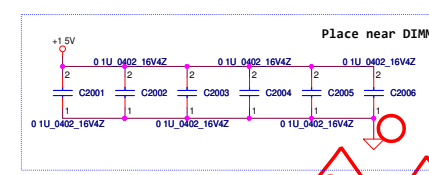


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Date: Tuesday, March 12, 2013				Sheet	9 of 51
Rev				1.0	

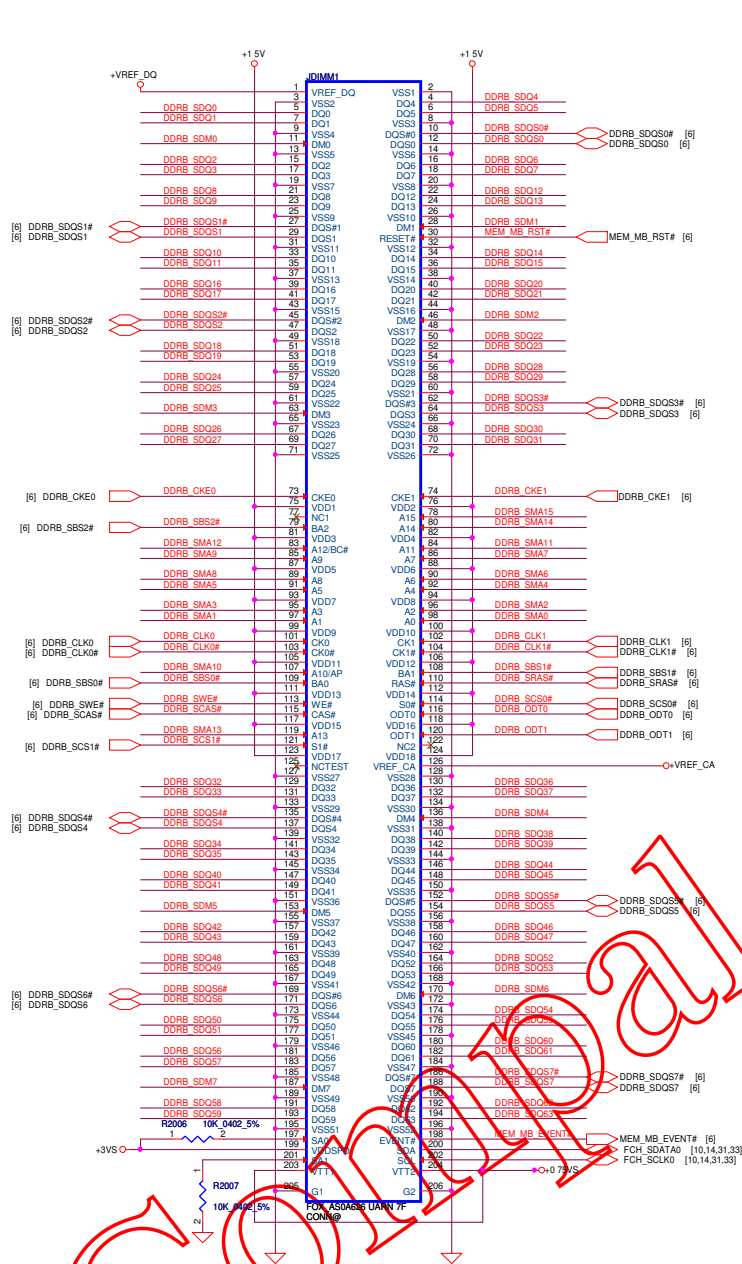
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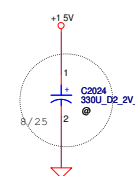
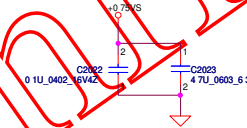
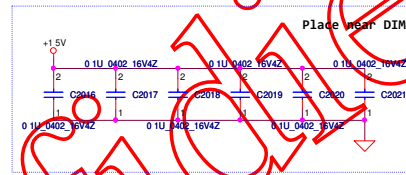
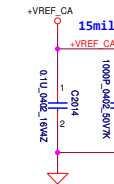
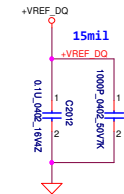
DDRA\_SDQ0 63# DDRA\_SDQ0 63# [6]  
 DDRA\_SDM0 71 DDRA\_SDM0 71 [6]  
 DDRA\_SMA0 15 DDRA\_SMA0 15 [6]



Reverse H:5.2mm



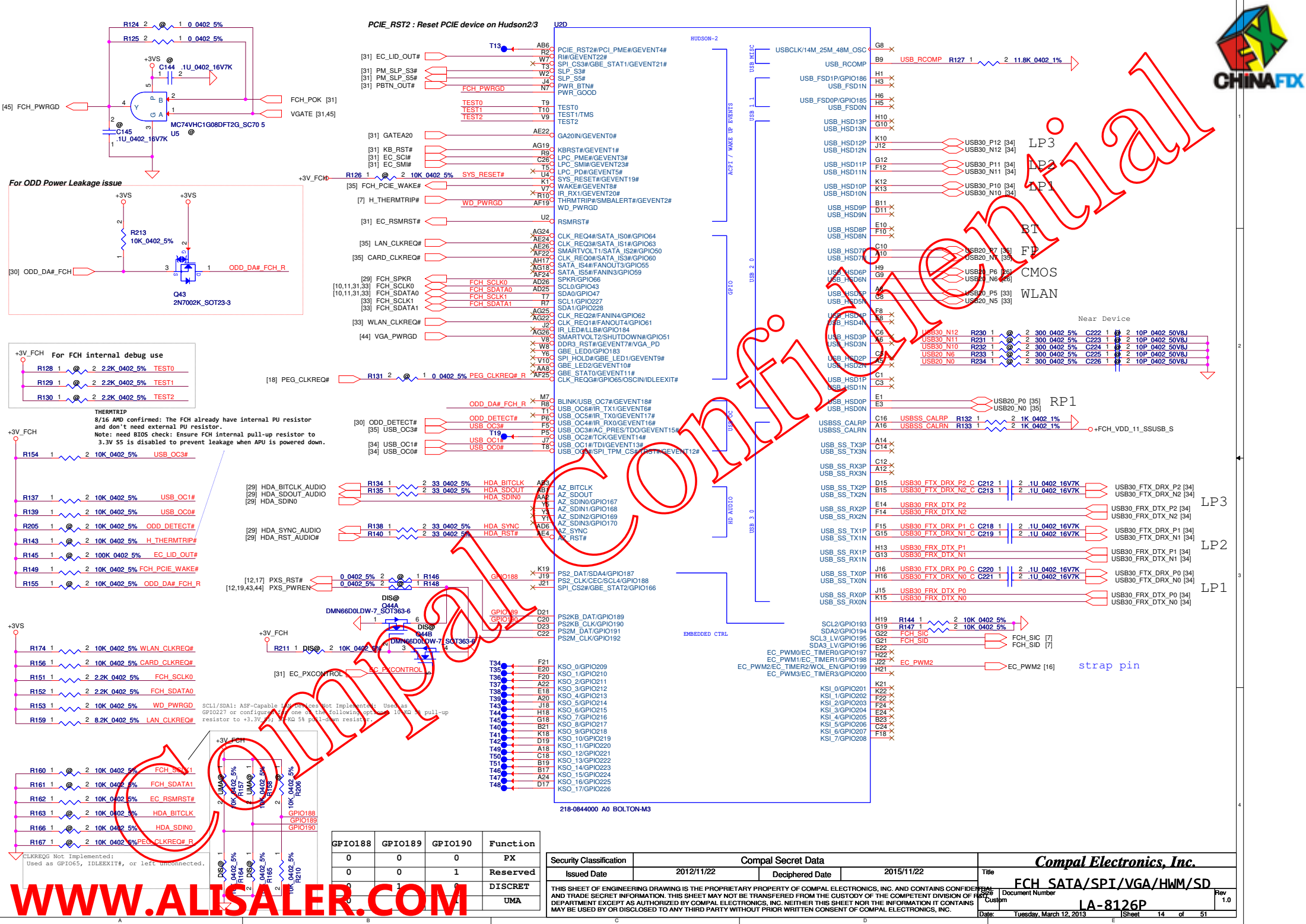
DDR8\_SDO[0:63] DDR8\_SDO[0:63] [6]  
 DDR8\_SDM[0:7] DDR8\_SDM[0:7] [6]  
 DDR8\_SMA[0:15] DDR8\_SMA[0:15] [6]

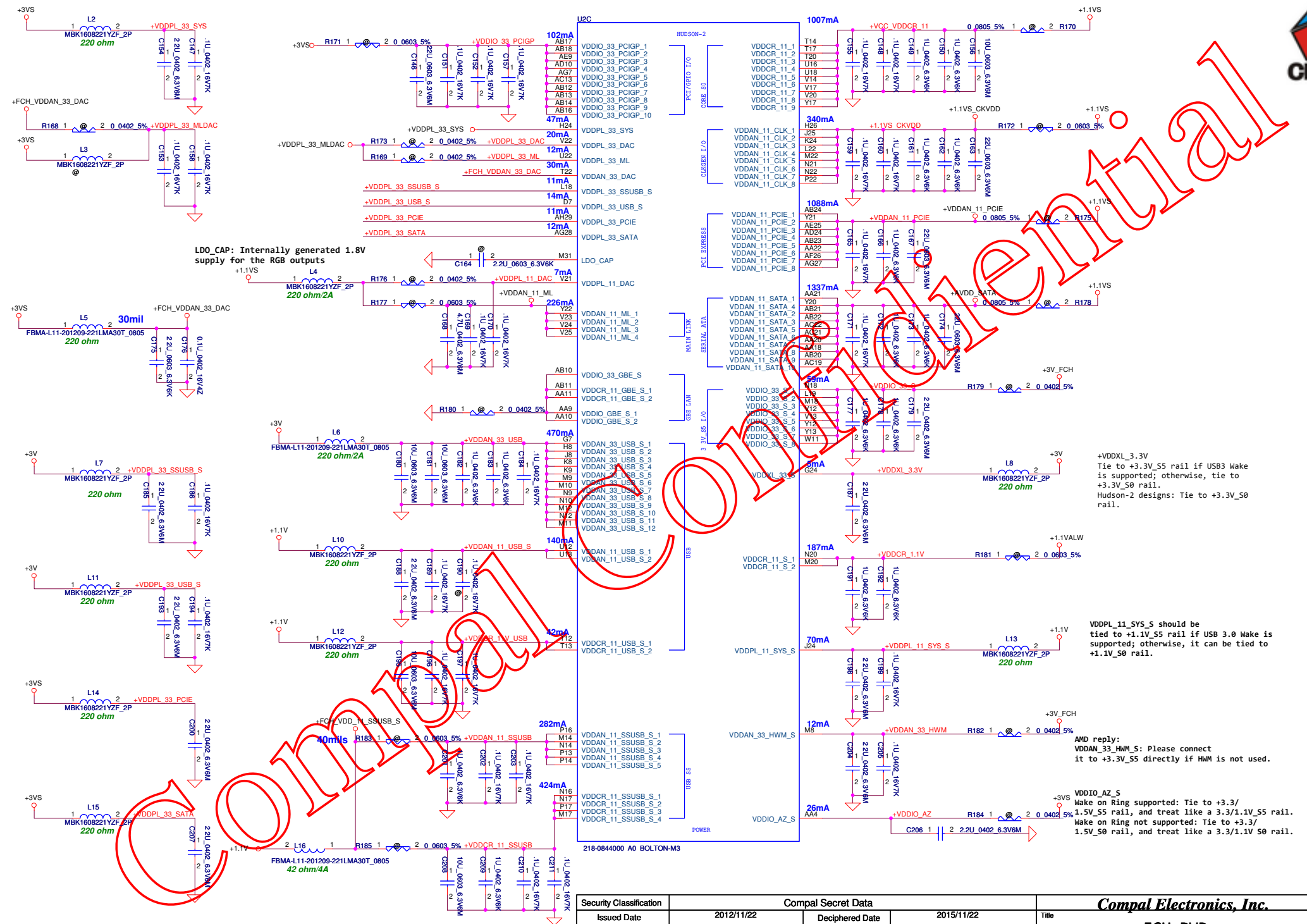






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					Doc Number	
					Custom	
					Rev 1.0	
Date: Tuesday, March 12, 2013					Sheet 13 of 51	
					LA-8126P	





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						File No.		Document Number		Rev	
						Custom		LA-8126P		1.0	
						Date:		Tuesday, March 12, 2013		Sheet 15 of 51	

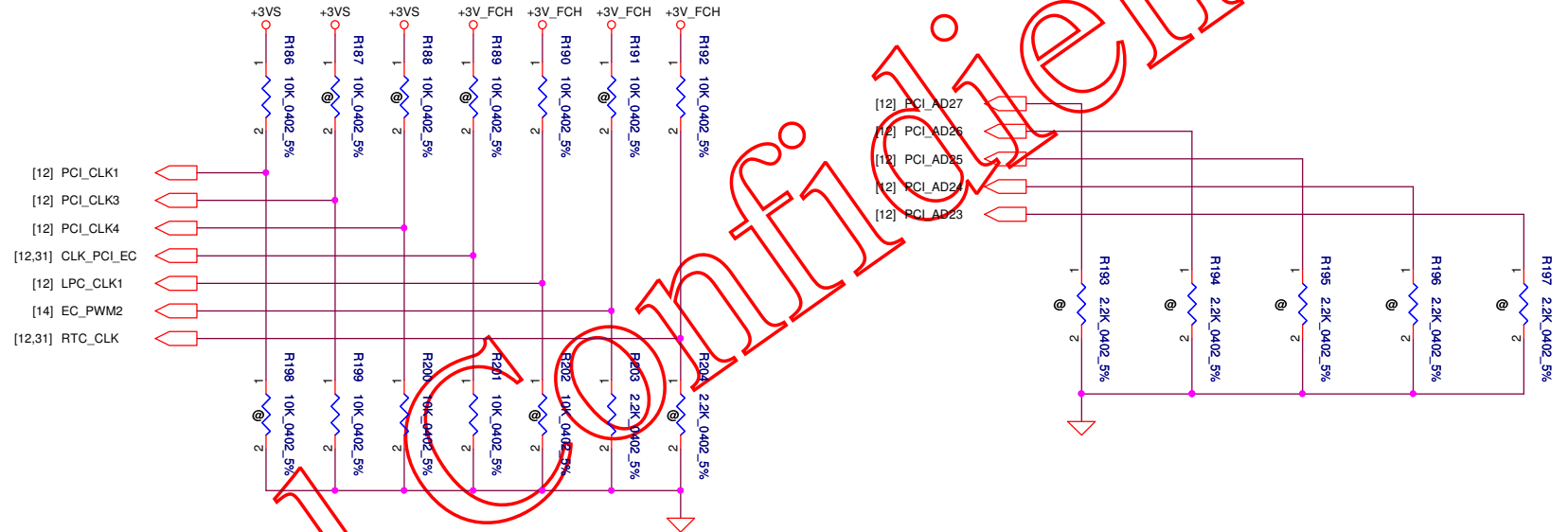
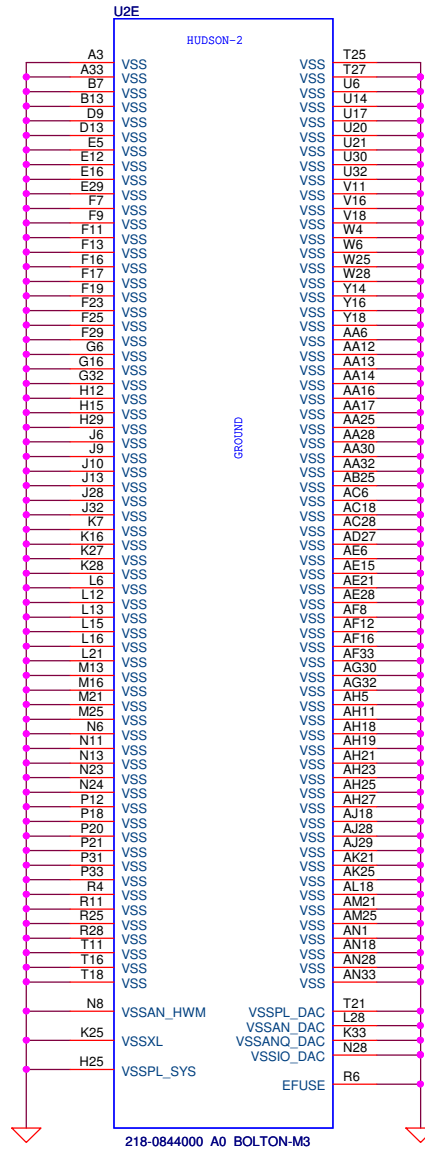
## STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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				Rev 1.0
				Date: Tuesday, March 12, 2013
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[5] PCIE\_CTX\_GRX\_P[7..0] → PCIE\_CTX\_GRX\_P[7..0]  
 [5] PCIE\_CTX\_GRX\_N[7..0] → PCIE\_CTX\_GRX\_N[7..0]

PCIE\_CRX\_GTX\_P[7..0] → PCIE\_CRX\_GTX\_P[7..0] [5]  
 PCIE\_CRX\_GTX\_N[7..0] → PCIE\_CRX\_GTX\_N[7..0] [5]

SDV/FVT, NO.3  
 U1401A

PART 1 OF 9

PCIE\_CTX\_GRX\_P0 AA38  
 PCIE\_CTX\_GRX\_N0 Y37  
 PCIE\_CTX\_GRX\_P1 Y35  
 PCIE\_CTX\_GRX\_N1 W36  
 PCIE\_CTX\_GRX\_P2 W38  
 PCIE\_CTX\_GRX\_N2 V37  
 PCIE\_CTX\_GRX\_P3 V35  
 PCIE\_CTX\_GRX\_N3 U36  
 PCIE\_CTX\_GRX\_P4 U38  
 PCIE\_CTX\_GRX\_N4 T37  
 PCIE\_CTX\_GRX\_P5 T35  
 PCIE\_CTX\_GRX\_N5 R36  
 PCIE\_CTX\_GRX\_P6 R38  
 PCIE\_CTX\_GRX\_N6 P37  
 PCIE\_CTX\_GRX\_P7 P35  
 PCIE\_CTX\_GRX\_N7 N36

PCIE\_RX0P  
 PCIE\_RX0N  
 PCIE\_RX1P  
 PCIE\_RX1N  
 PCIE\_RX2P  
 PCIE\_RX2N  
 PCIE\_RX3P  
 PCIE\_RX3N  
 PCIE\_RX4P  
 PCIE\_RX4N  
 PCIE\_RX5P  
 PCIE\_RX5N  
 PCIE\_RX6P  
 PCIE\_RX6N  
 PCIE\_RX7P  
 PCIE\_RX7N

Y33 PCIE\_CRX\_C GTX\_P0 .1U 0402 16V7K 2 1 C1401 DIS@ PCIE\_CRX\_GTX\_P0  
 Y32 PCIE\_CRX\_C GTX\_N0 .1U 0402 16V7K 2 1 C1402 DIS@ PCIE\_CRX\_GTX\_N0  
 W33 PCIE\_CRX\_C GTX\_P1 .1U 0402 16V7K 2 1 C1404 DIS@ PCIE\_CRX\_GTX\_P1  
 W32 PCIE\_CRX\_C GTX\_N1 .1U 0402 16V7K 2 1 C1405 DIS@ PCIE\_CRX\_GTX\_N1  
 U33 PCIE\_CRX\_C GTX\_P2 .1U 0402 16V7K 2 1 C1406 DIS@ PCIE\_CRX\_GTX\_P2  
 U32 PCIE\_CRX\_C GTX\_N2 .1U 0402 16V7K 2 1 C1407 DIS@ PCIE\_CRX\_GTX\_N2  
 U30 PCIE\_CRX\_C GTX\_P3 .1U 0402 16V7K 2 1 C1408 DIS@ PCIE\_CRX\_GTX\_P3  
 U29 PCIE\_CRX\_C GTX\_N3 .1U 0402 16V7K 2 1 C1403 DIS@ PCIE\_CRX\_GTX\_N3  
 T33 PCIE\_CRX\_C GTX\_P4 .1U 0402 16V7K 2 1 C1409 DIS@ PCIE\_CRX\_GTX\_P4  
 T32 PCIE\_CRX\_C GTX\_N4 .1U 0402 16V7K 2 1 C1410 DIS@ PCIE\_CRX\_GTX\_N4  
 T30 PCIE\_CRX\_C GTX\_P5 .1U 0402 16V7K 2 1 C1411 DIS@ PCIE\_CRX\_GTX\_P5  
 T29 PCIE\_CRX\_C GTX\_N5 .1U 0402 16V7K 2 1 C1412 DIS@ PCIE\_CRX\_GTX\_N5  
 P33 PCIE\_CRX\_C GTX\_P6 .1U 0402 16V7K 2 1 C1413 DIS@ PCIE\_CRX\_GTX\_P6  
 P32 PCIE\_CRX\_C GTX\_N6 .1U 0402 16V7K 2 1 C1414 DIS@ PCIE\_CRX\_GTX\_N6  
 P30 PCIE\_CRX\_C GTX\_P7 .1U 0402 16V7K 2 1 C1415 DIS@ PCIE\_CRX\_GTX\_P7  
 P29 PCIE\_CRX\_C GTX\_N7 .1U 0402 16V7K 2 1 C1416 DIS@ PCIE\_CRX\_GTX\_N7

SDV/FVT, NO.2

SDV/FVT, NO.1

N38 X NC  
 M37 X NC  
 M35 X NC  
 L36 X NC  
 L38 X NC  
 K37 X NC  
 K35 X NC  
 J36 X NC  
 J38 X NC  
 H37 X NC  
 H35 X NC  
 G36 X NC  
 G38 X NC  
 F37 X NC  
 F35 X NC  
 E37 X NC

PCI EXPRESS INTERFACE

NC X N33  
 NC X N32  
 NC X N30  
 NC X N29  
 NC X L33  
 NC X L32  
 NC X L30  
 NC X L29  
 NC X K33  
 NC X K32  
 NC X J33  
 NC X J32  
 NC X K30  
 NC X K29  
 NC X H33  
 NC X H32

CLOCK

[12] CLK\_PCIE\_VGA → CLK\_PCIE\_VGA# AB35  
 [12] CLK\_PCIE\_VGA# → CLK\_PCIE\_VGA# AA36

TEST\_PG  
 GPU\_RST#  
 AA30  
 DIS@ R2486 100K 0402 5%

CALIBRATION

PCIE\_CALR\_TX Y30 R1404 1 DIS@ 2 1.69K 0402 1% → +0.95VGS  
 PCIE\_CALR\_RX Y30 R1405 1 DIS@ 2 1K 0402 1% → +0.95VGS

## LVDS Interface

U1401D

PART 7 OF 9

LVDS CONTROL

RSVD/VARY BL  
 RSVD/DIGON

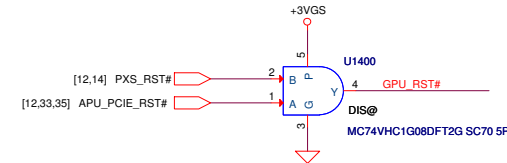
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 TXCBM\_DPB3N  
 TX3M\_DPB2N  
 TX4P\_DPB1P  
 TX4M\_DPB1N  
 TX5P\_DPB0P  
 TX5M\_DPB0N  
 NC#AF35  
 NC#AG36

TXCAP\_DPA3P  
 TXCAM\_DPA3N  
 TX0P\_DPA2P  
 TX0M\_DPA2N  
 TX1P\_DPA1P  
 TX1M\_DPA1N  
 TX2P\_DPA0P  
 TX2M\_DPA0N  
 NC  
 NC

AK27  
 AJ27  
 AK35  
 AL36  
 AJ38  
 AK37  
 AJ35  
 AJ36  
 AG38  
 AH37  
 AF35  
 AG36

AP34  
 AR34  
 AW37  
 AU35  
 AR37  
 AU39  
 AP35  
 AR35  
 AN36  
 AP37

DIS@ S IC 216-0841000 A0 SUN PRO M2 FCBGA 962P A39





# CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRNS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De emphasis Enable 0:Tx de emphasis disabled 1:Tx de emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped LOW)	1
BIF_VGA_DIS	PS_2[4]	0:GEN3 not support at power on 1:GEN3 supported at power on	0
ROMIDCFQ[2:0]	PS_0[3:1]	0:VGA control 1:G3A controller capacity enabled 2:G3A controller capacity disabled (for multi GPU)	XXX
BIOS_ROM_EN	PS_0[4]	0:Enable external BIOS ROM device 1:Disabled	X
AUD[1]	NA	00: No audio function 01: Audio for DP only 10: Audio for DP and HDMI if dongle is detected 11: Audio for both DP and HDMI	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

## Resistor Divider Lookup Table

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
R1430	R1436	
NC	NC	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

## Capacitor Divider Lookup Table

Cap (nF)	Bitd [5:4]	Compal PN
C1439		
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

## AVDD MarsCRB Design

Design	120ohm	0.1u	1u	10u
AVDD	1	1	1	1
MarsCRB	1	1	1	1

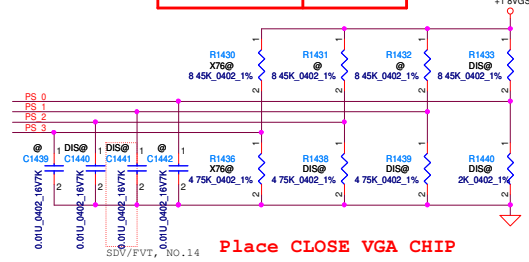
## VDDIDI MarsCRB Design

Design	120ohm	0.1u	1u	10u
VDDIDI	1	1	1	1
MarsCRB	1	1	1	1

## MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

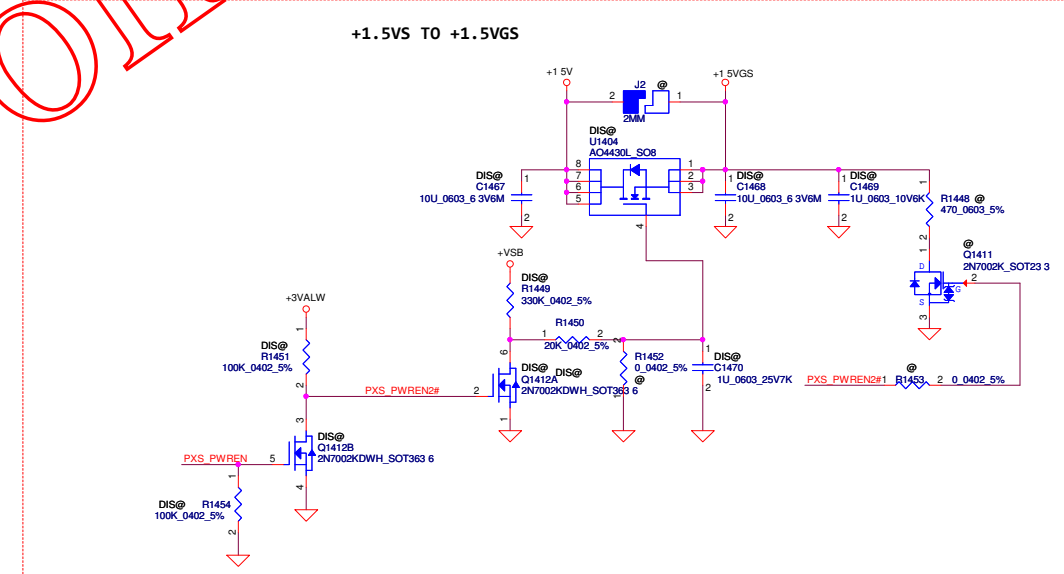
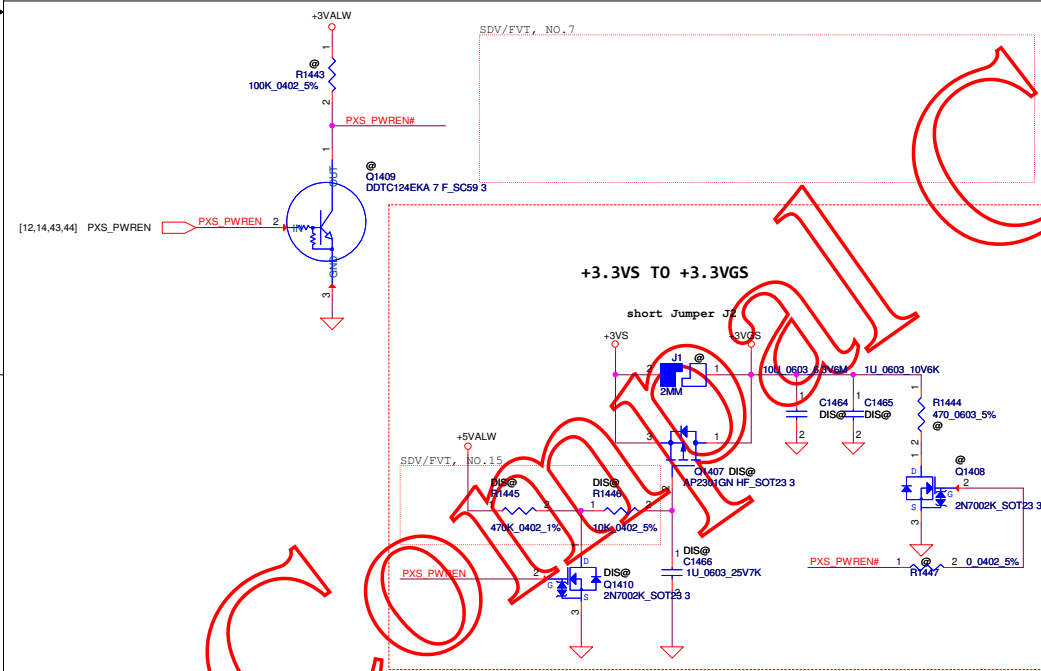
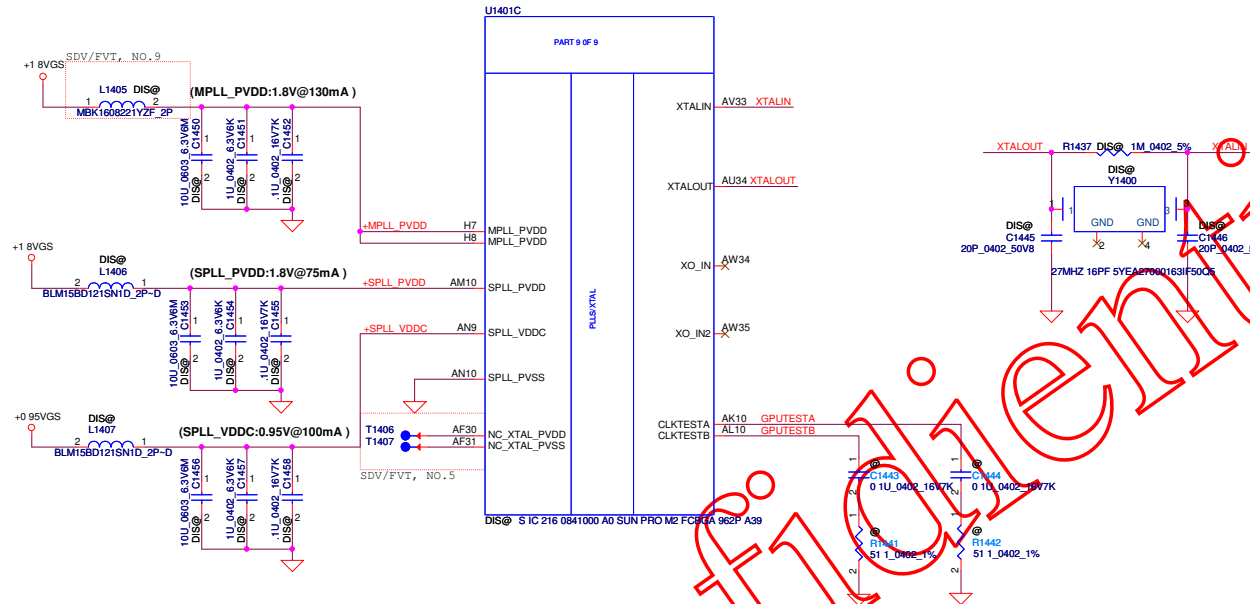
Mapping to VRAM type please refer to page 04



MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

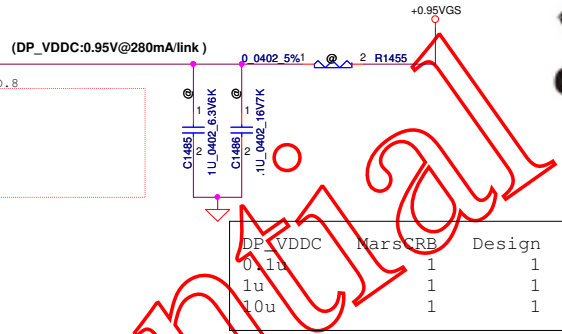
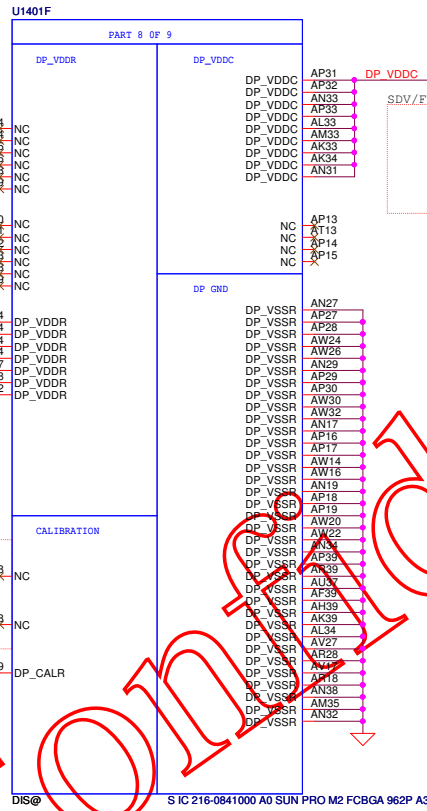
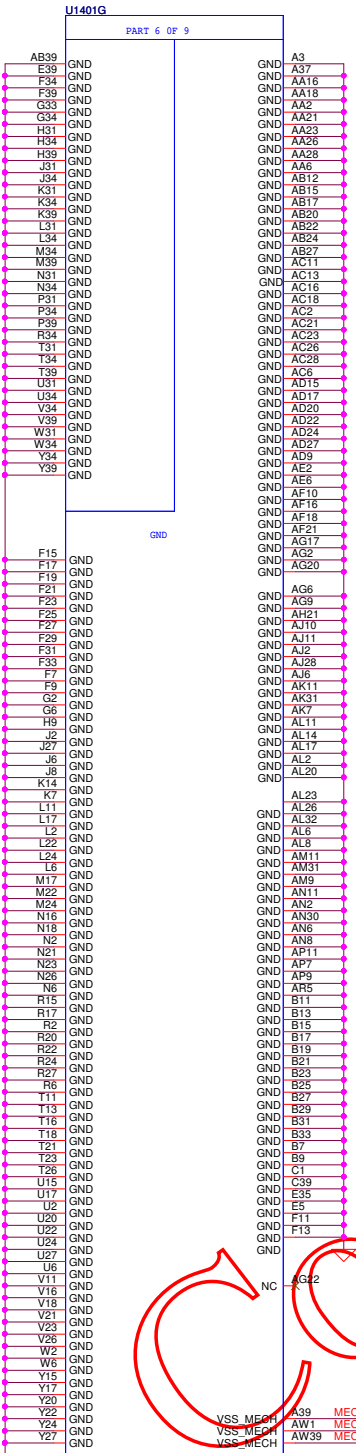
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



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DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

AMD:  
no display from GPU,  
can uninstall the capacitors

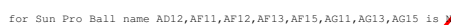


DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

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PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



Route as differential pair

○

VD  
VD

M23



11

10

11

10

10

11

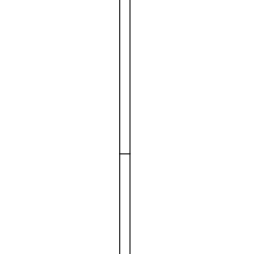
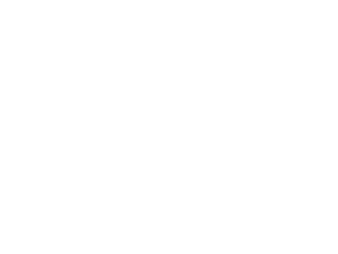
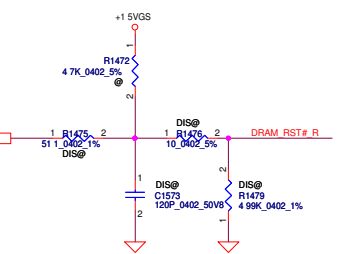
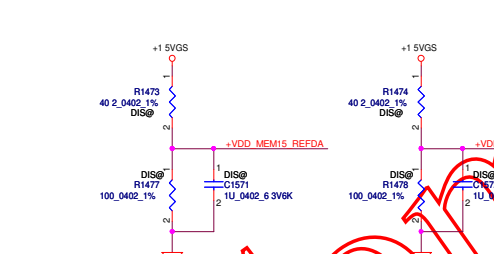
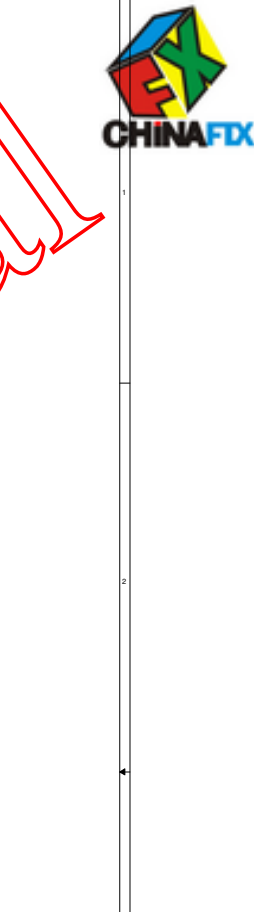
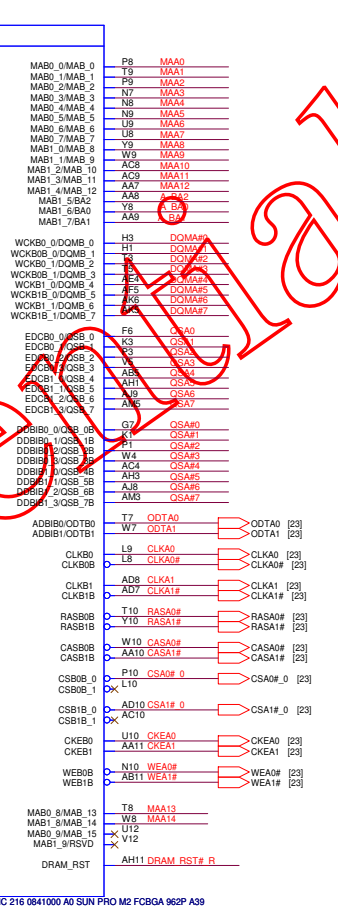
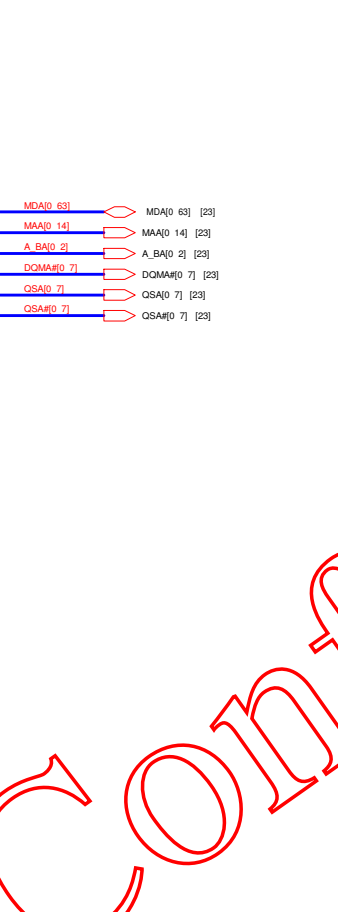
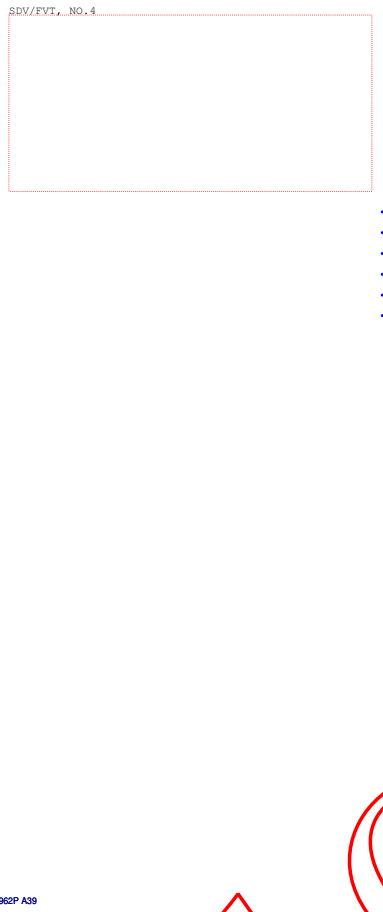
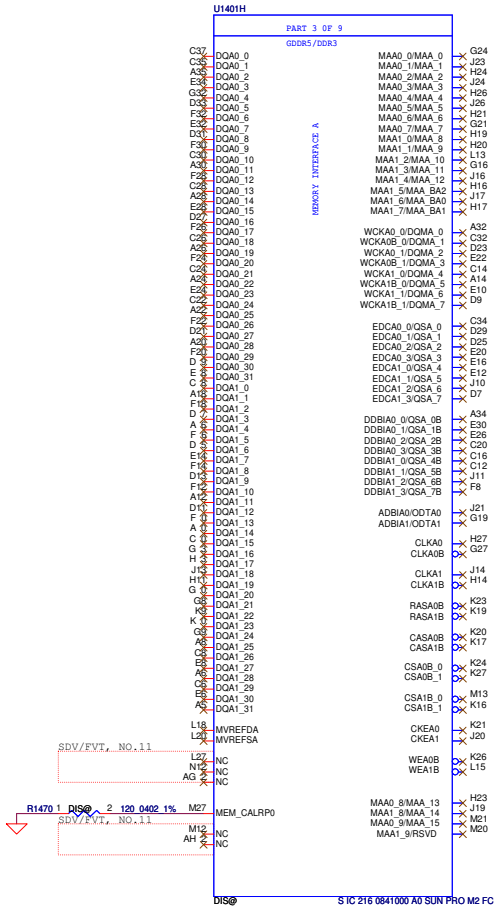
10

100 DI

221 DI

100

DIS@ S IC 216 0841000 A0 SUN PRO M2 FCBGA 962P A39

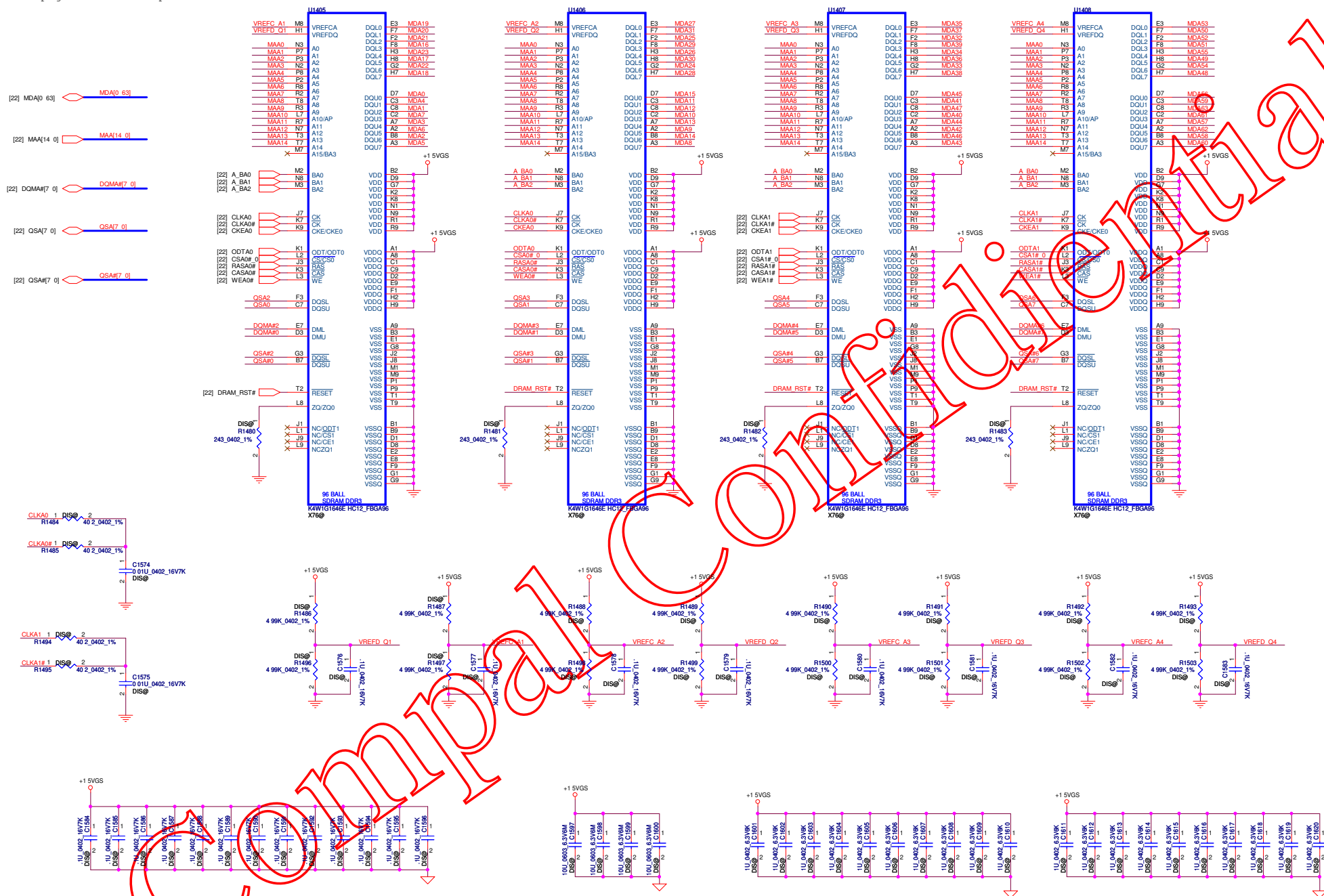


**DRAM\_RST# is a daisy-chain net that connects to all VRAM**

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

The Seymour M2 only support channel B (64 bit),  
this page unmount all parts



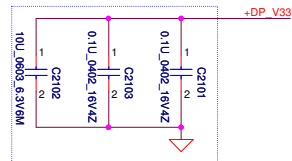


Compal Confidential

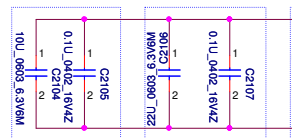
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2015/11/22	
2012/11/22		2015/11/22		ATT Sun Pro_M2_VRAM_B	
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		C		LA-8126P	10
		Date:		Tuesday, March 12, 2013	Sheet 24 of 51



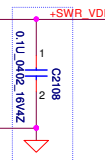
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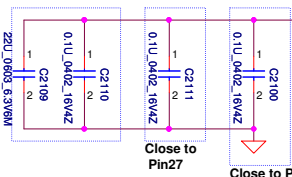
Close to L27



Close to Pin18



Close to L29

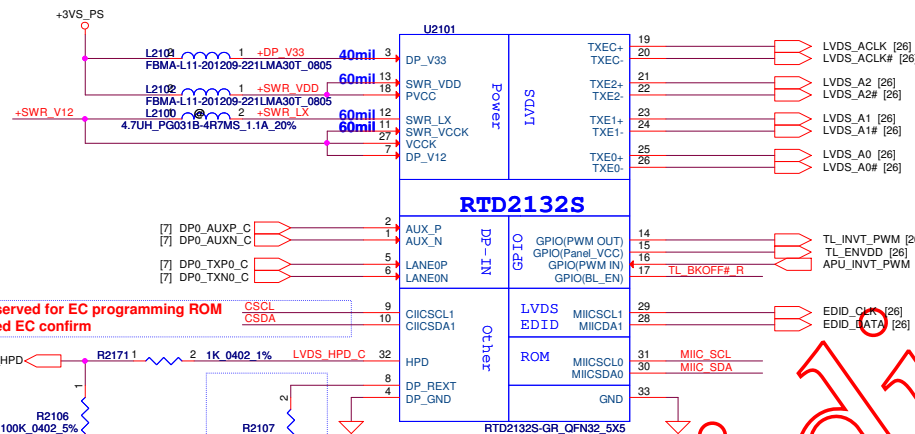


Close to Pin27

Close to Pin7

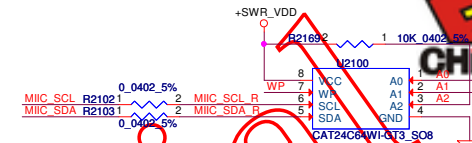
Part number: SA00004EU10

EEROM

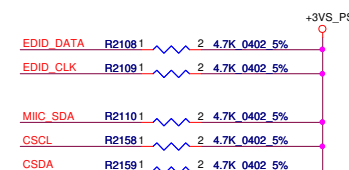


Reserved for EC programming ROM  
Need EC confirm

Change to 12Kohm 1% (DG ref.)  
20101114

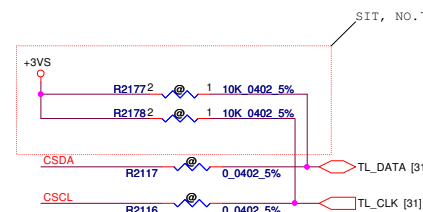
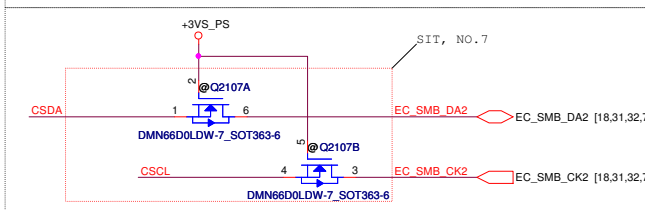
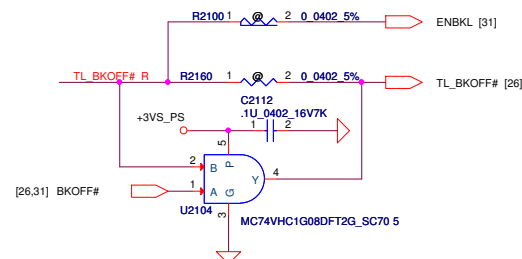


2132S-Ver E: External ROM, pin31 PU +3VS  
Internal RAM support, pin31 PD to GND  
EEROM EEROM EEROM EEROM



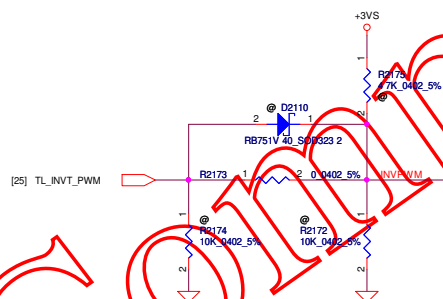
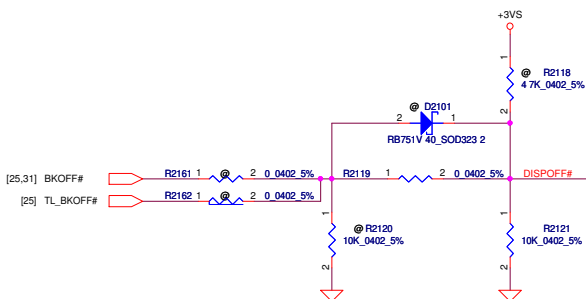
Vendor Suggest 2011.08.15

Vendor advise reserve it

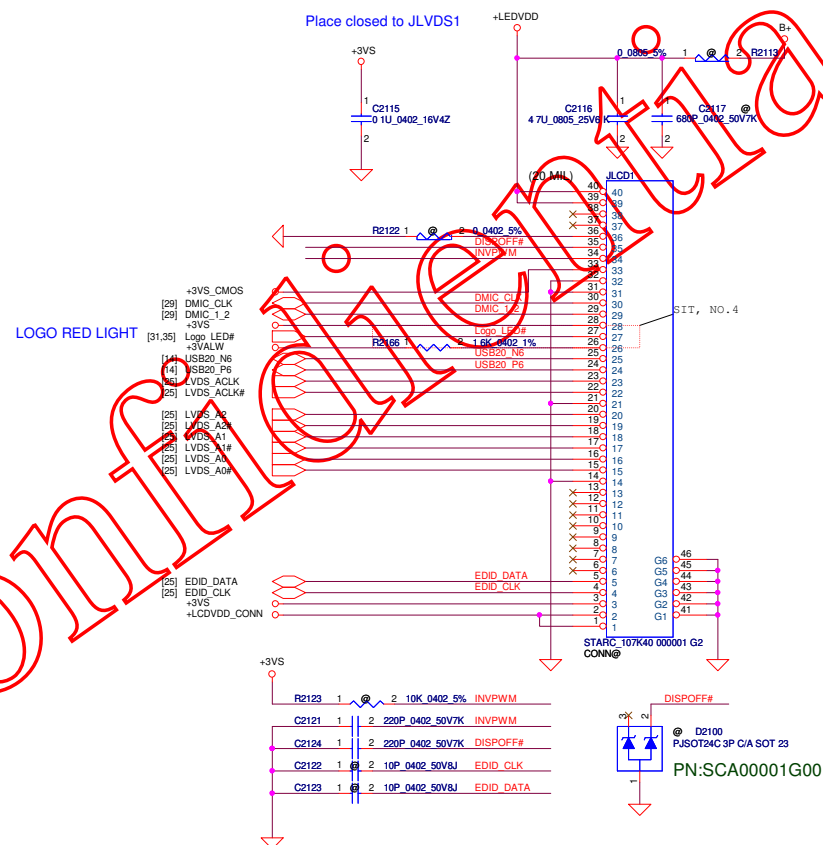


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Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	LVDS Translator - RTD2132S
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				Date	Tuesday, March 12, 2013
				Sheet	25 of 51

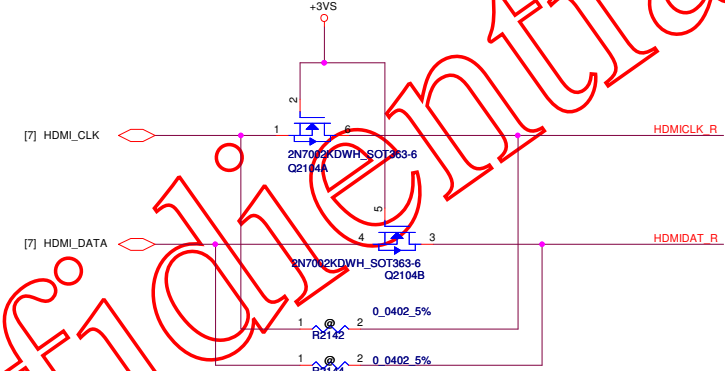
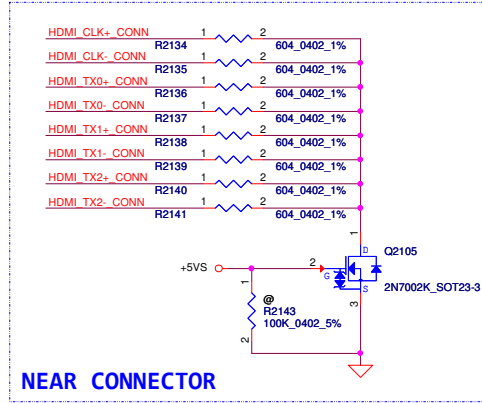
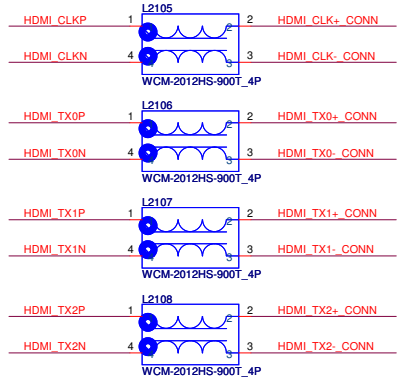


Place closed to JLVDS1

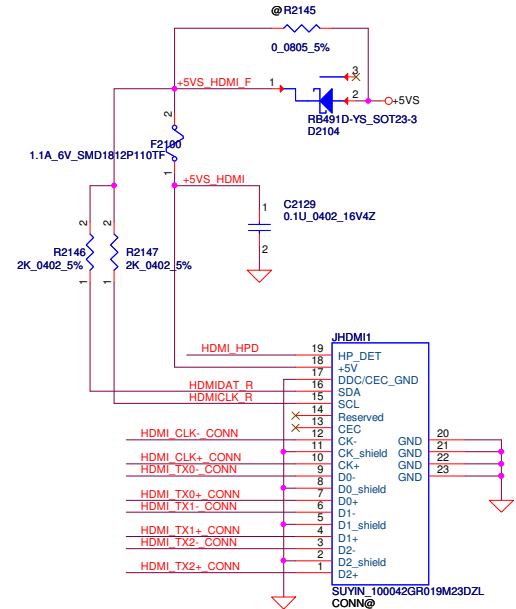
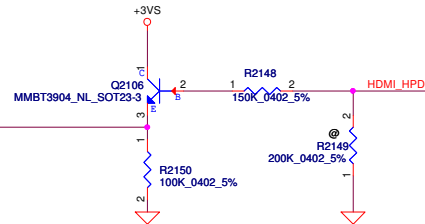
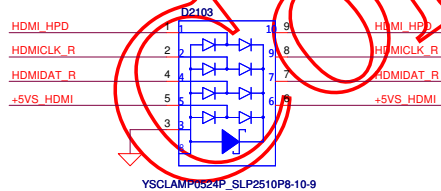
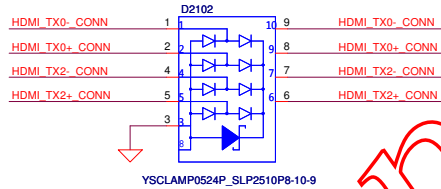
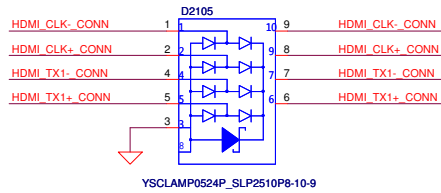


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>				
Issued Date		2012/11/22	Deciphered Date	2015/11/22		Title		
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						Size	Document Number	Rev
						Custn	LA-8126P	
Date		Tuesday, March 12, 2013		Sheet	26	of 51		

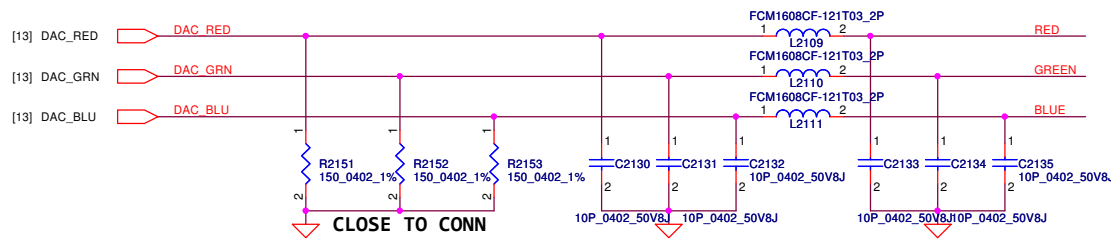
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[7] HDMI_CLKN	R2127	1	2	0	0402_5%	HDMI_CLK-_CONN
[7] HDMI_TX0P	R2128	1	2	0	0402_5%	HDMI_TX0+_CONN
[7] HDMI_TX0N	R2129	1	2	0	0402_5%	HDMI_TX0-_CONN
[7] HDMI_TX1P	R2130	1	2	0	0402_5%	HDMI_TX1+_CONN
[7] HDMI_TX1N	R2131	1	2	0	0402_5%	HDMI_TX1-_CONN
[7] HDMI_TX2P	R2132	1	2	0	0402_5%	HDMI_TX2+_CONN
[7] HDMI_TX2N	R2133	1	2	0	0402_5%	HDMI_TX2-_CONN



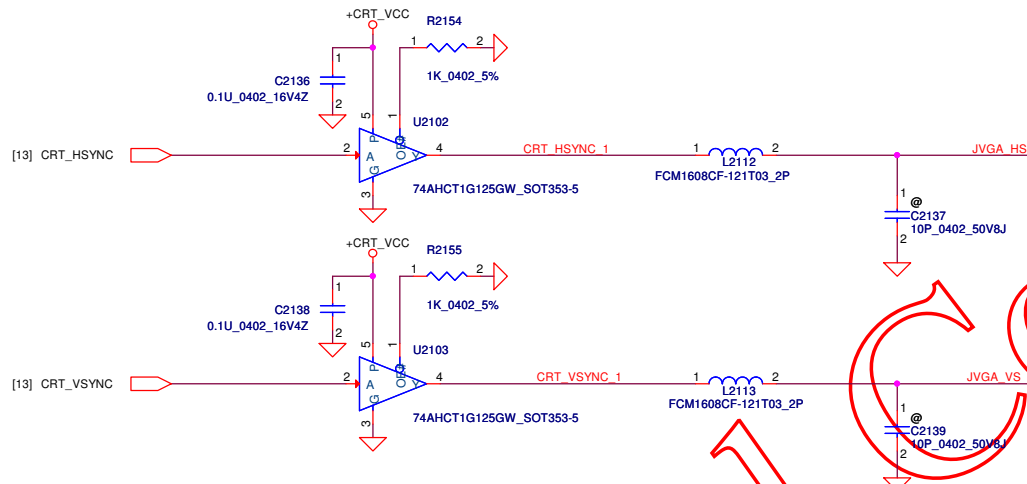
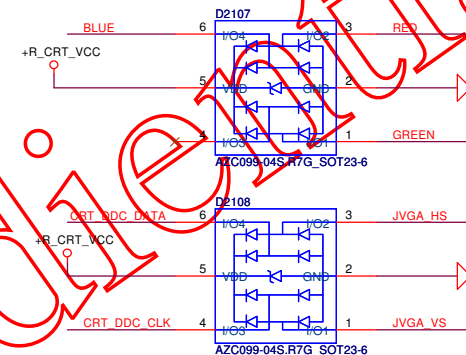
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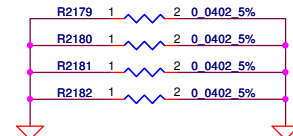
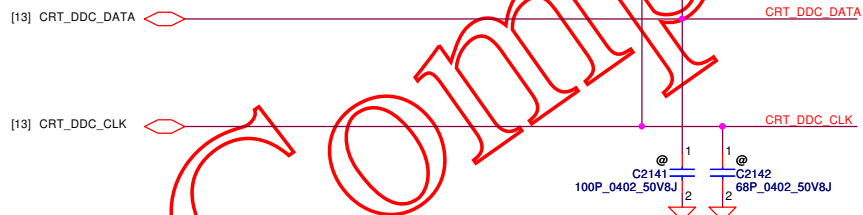
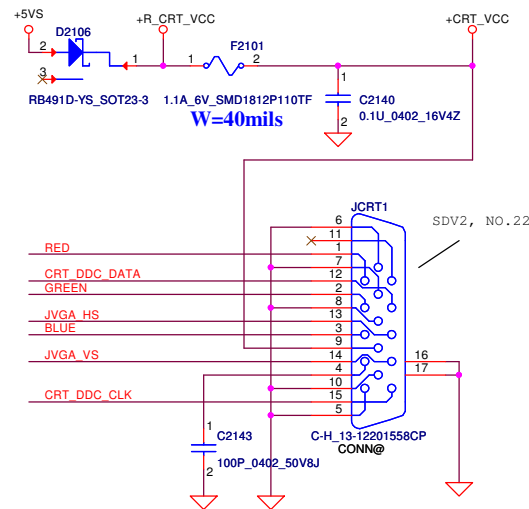
Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	HDMI Connector	
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				LA-8126P	
				Date: Tuesday, March 12, 2013	Sheet 27 of 51



## ESD Request



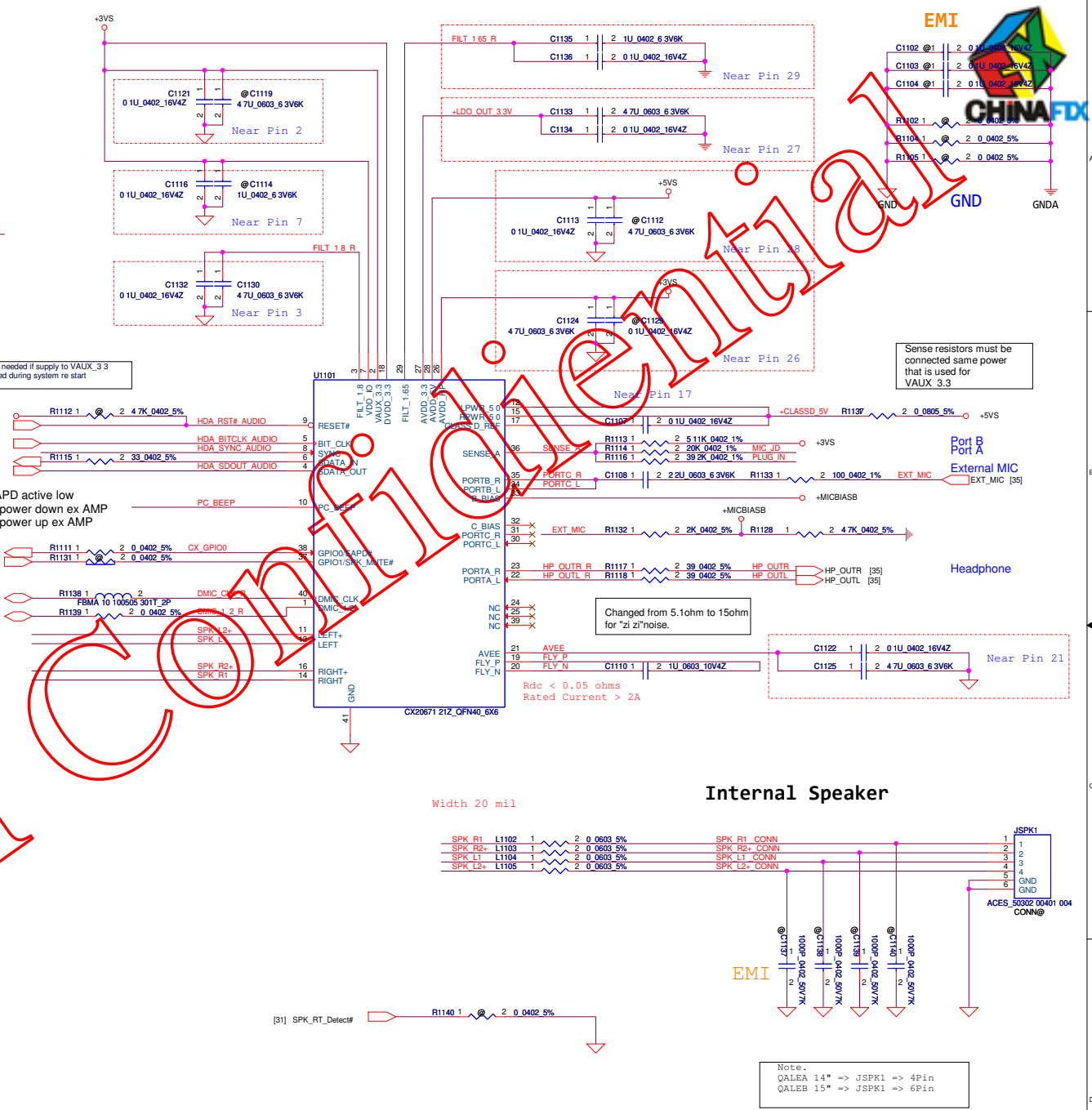
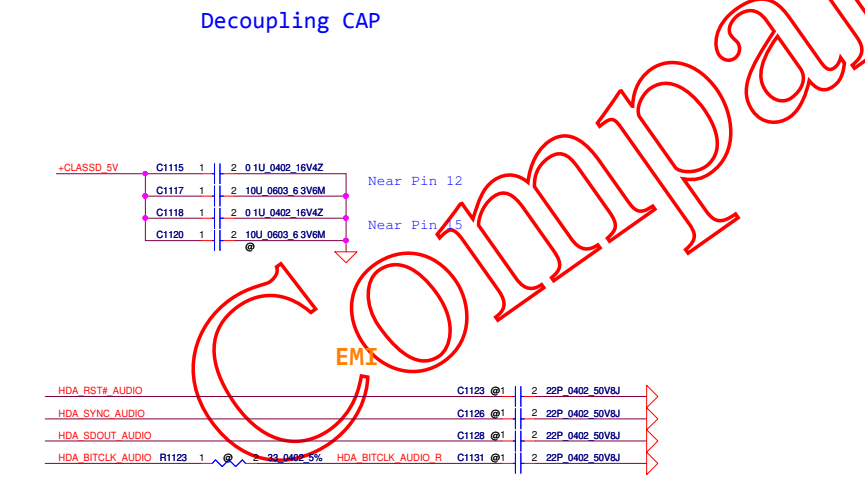
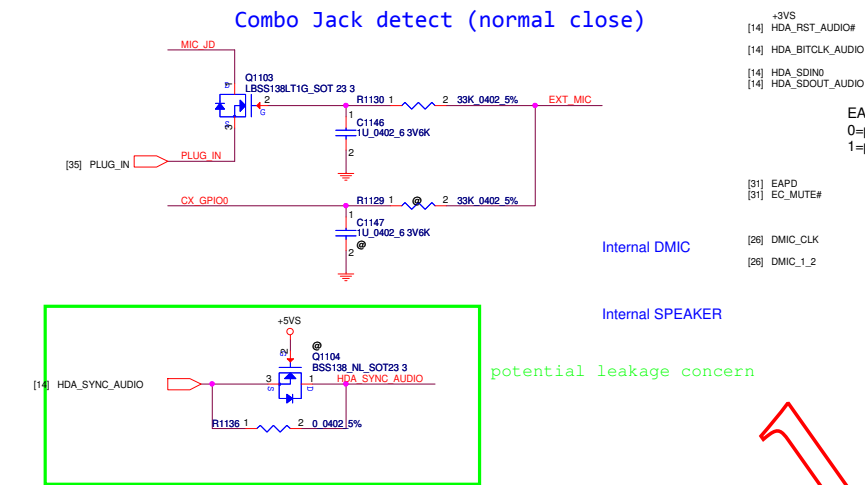
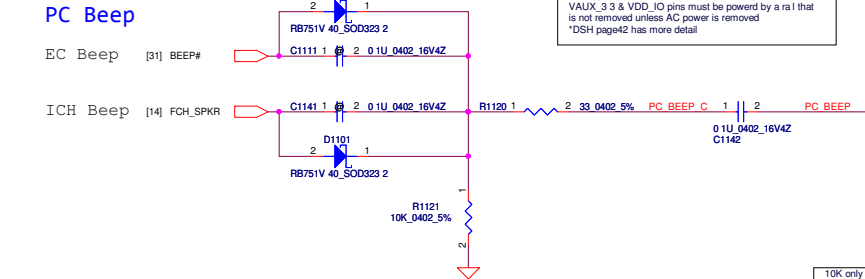
## CRT Connector



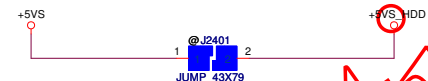
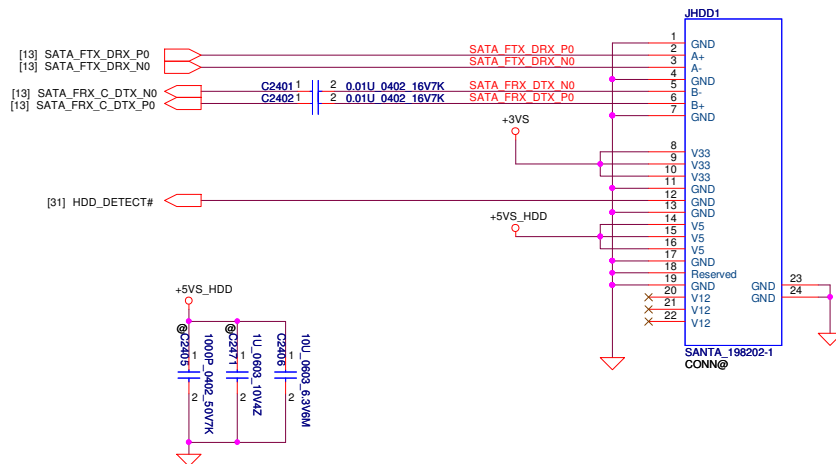
AMD check list update  
20101110

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Issued Date		2012/11/22		Deciphered Date		2015/11/22	
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						CRT Connector	
Size		Document Number				Rev	
Custom		LA-8126P				1.0	
Date:		Tuesday, March 12, 2013		Sheet		28 of 51	

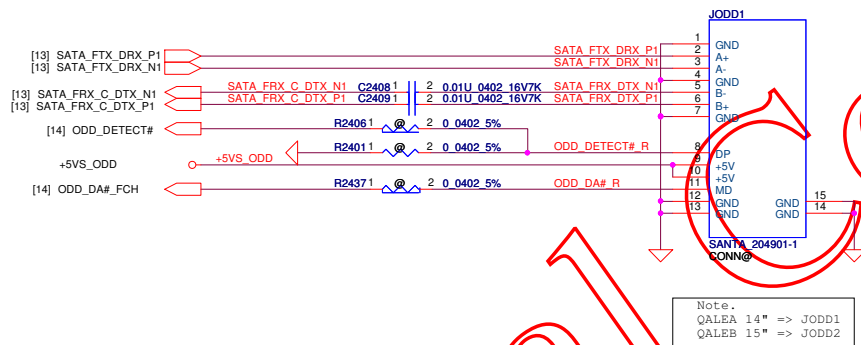
CX20671  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.  
An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).



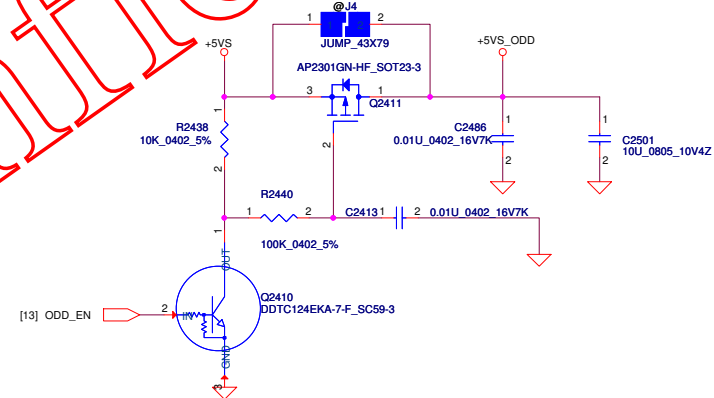
## SATA HDD Conn.



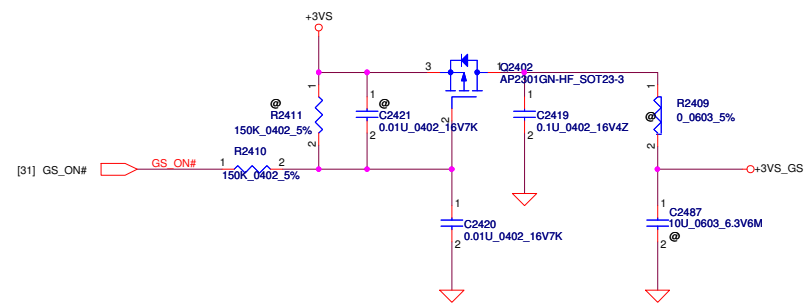
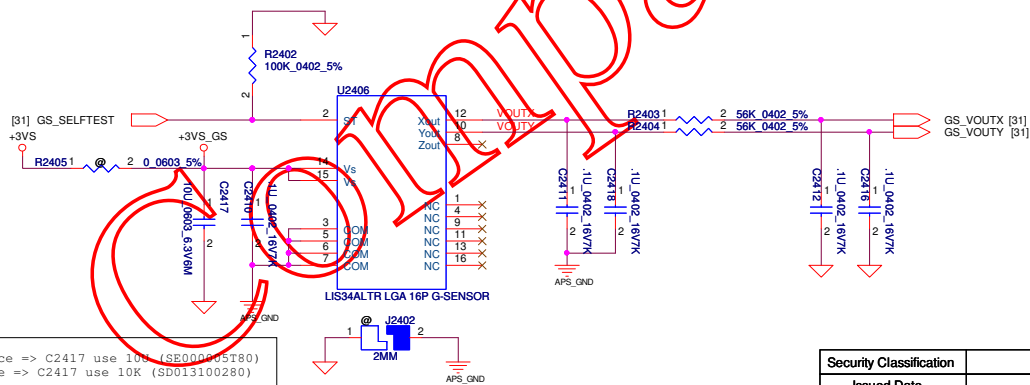
## SATA ODD Conn.



## ODD Power Control



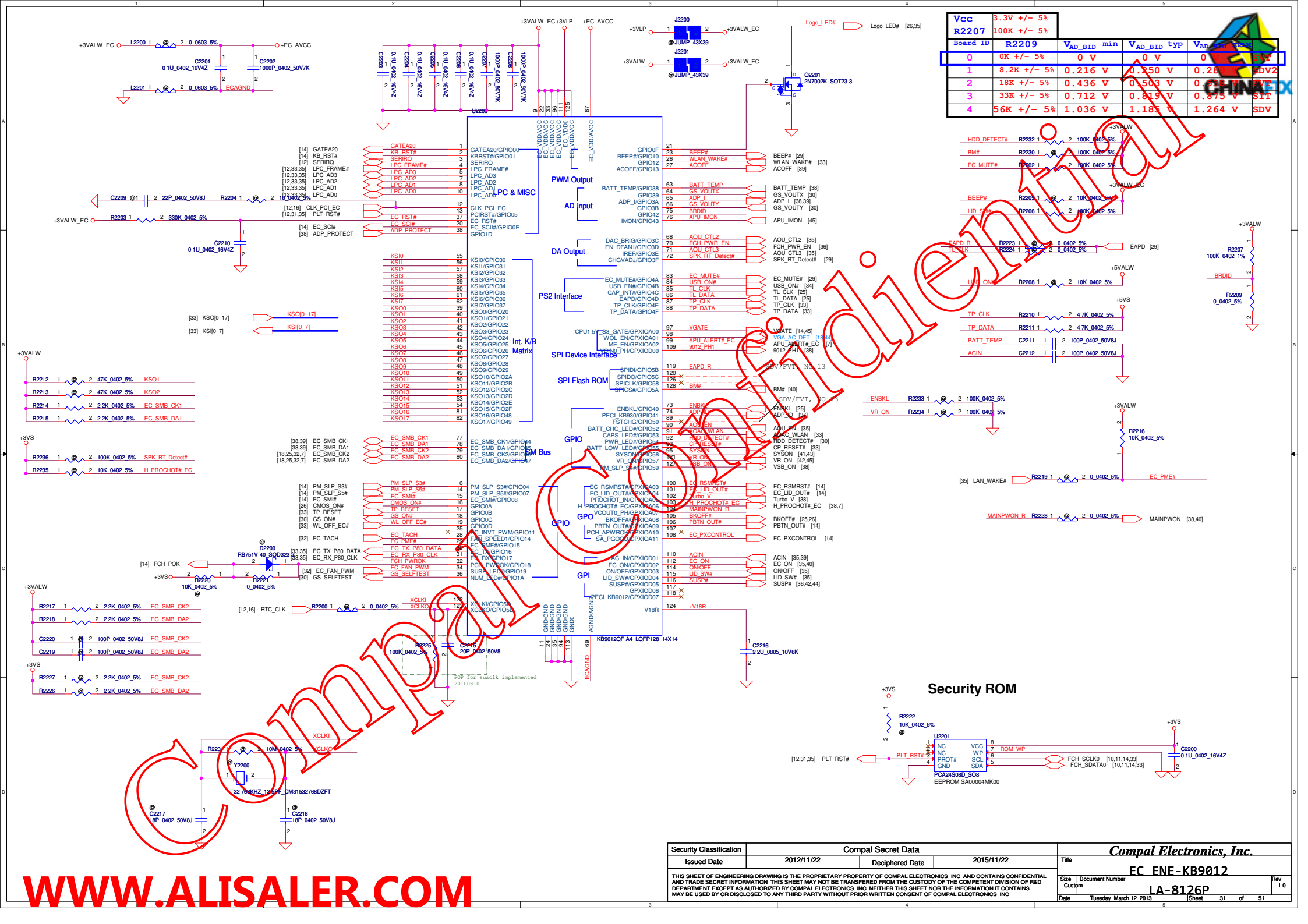
## APS G-Sensor



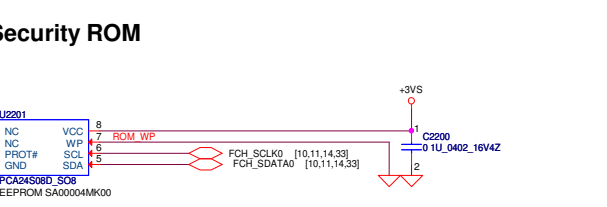
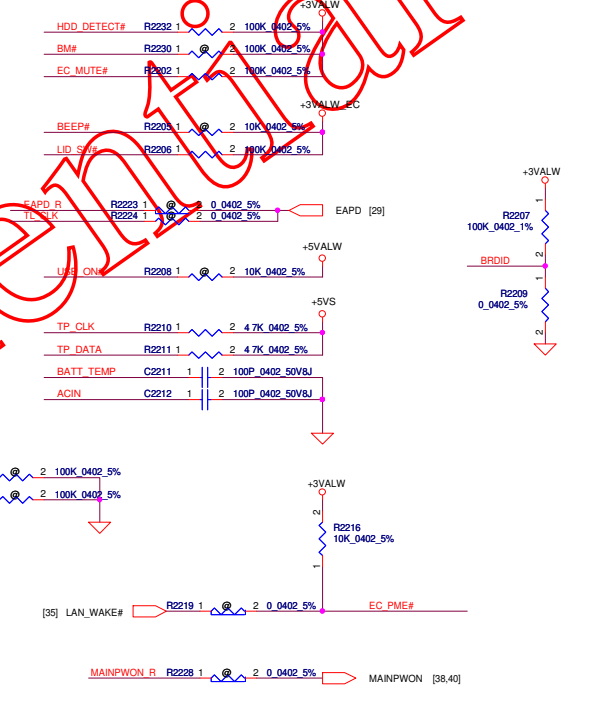
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Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	HDD/ODD/G-Sensor	
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				LA-8126P	
				Date: Tuesday, March 12, 2013	Sheet 30 of 51



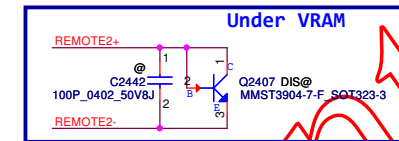
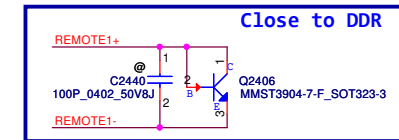
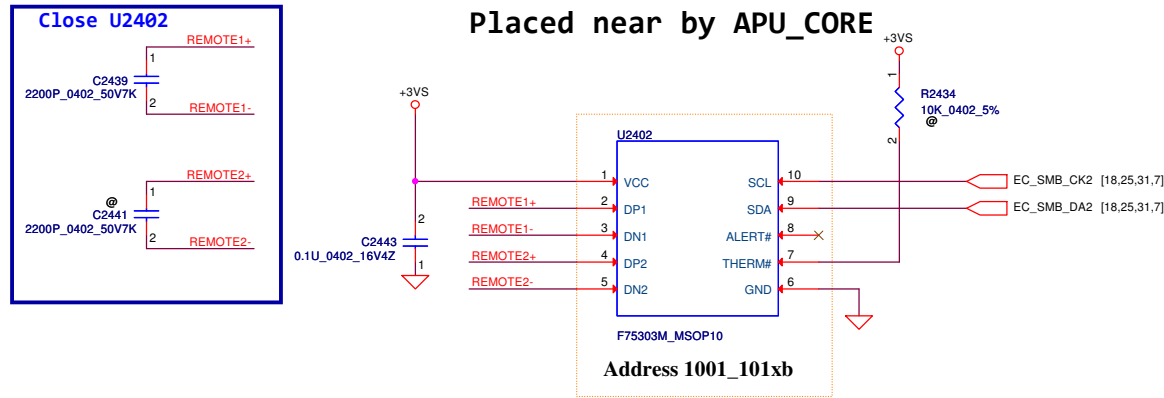


Vcc	3.3V +/- 5%				
R2207	100K +/- 5%				
Board ID	R2209	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.28 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SDV



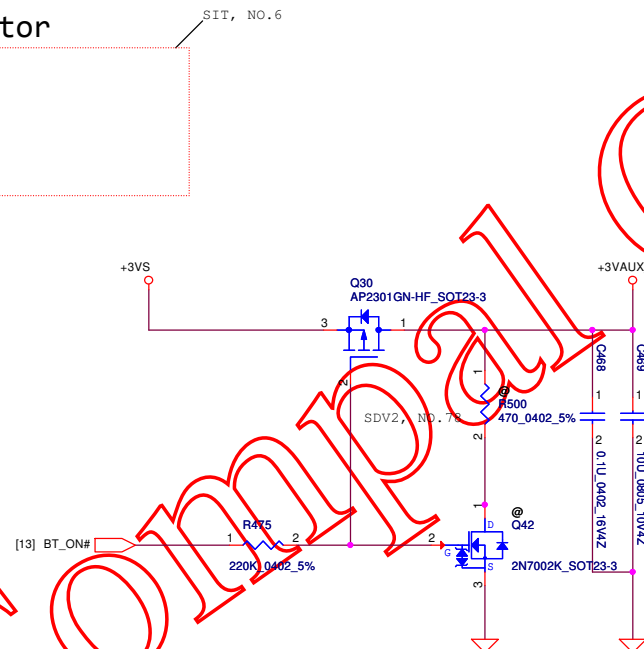
Security Classification	Compal Secret Data
Issued Date	2012/11/22
Deciphered Date	2015/11/22
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Title	
EC FNE-KB9012	
Rev 0	
Date	
Tuesday, March 12, 2013	
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# Fintek Thermal sensor Placed near by APU\_CORE

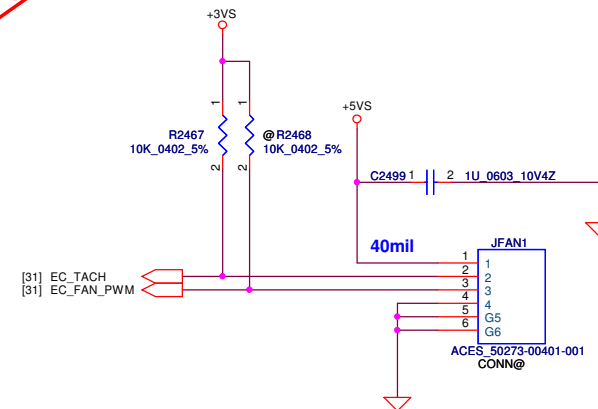


REMOTE1-2+/-:  
Trace width/spacer:10/10 mil  
Trace length:<8"

## BT Connector



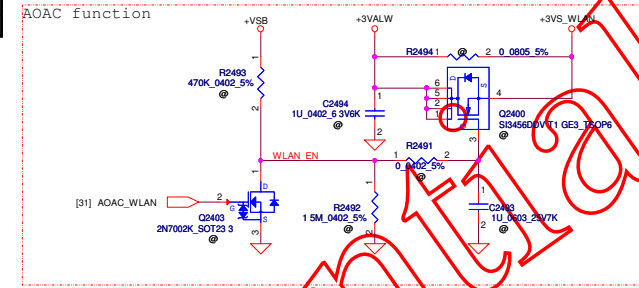
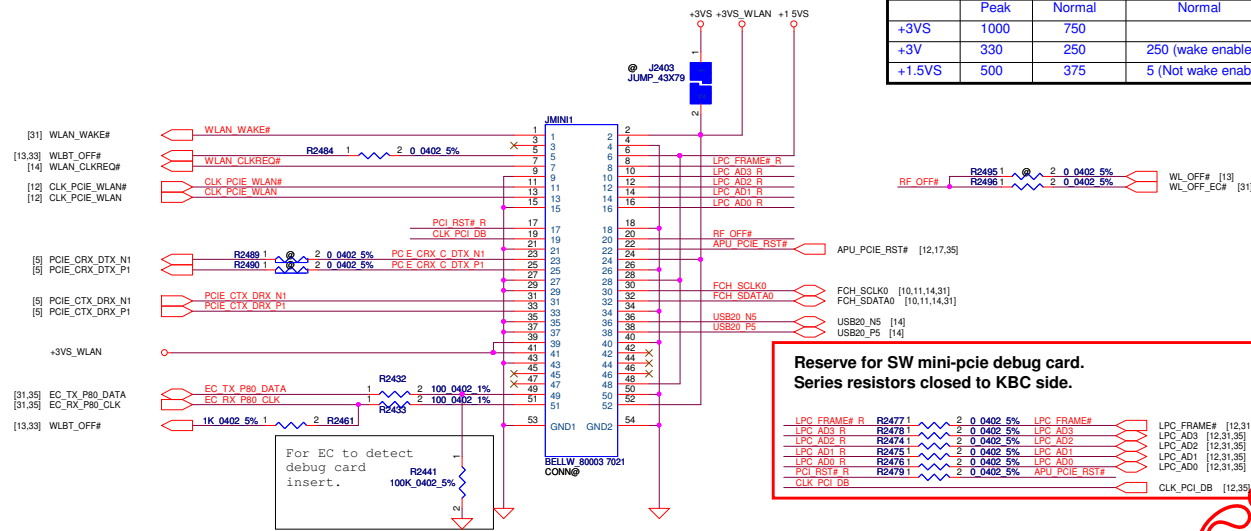
## FAN1 Conn



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				LA-8126P	
				Date	Rev
				Tuesday, March 12, 2013	1.0
				Sheet	32 of 51

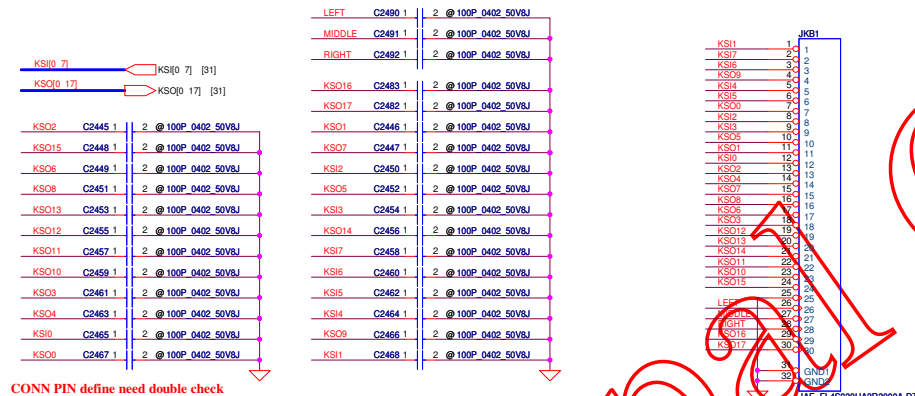
## WLAN Conn

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

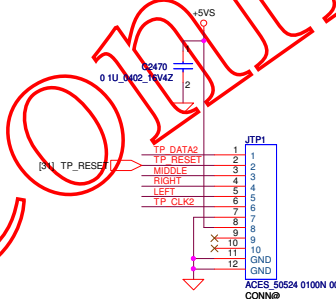


For AOAC assessment  
+3VS\_WLAN path:  
1. +3VS (default)  
2. +3VALW  
3. +3VALW + Switch

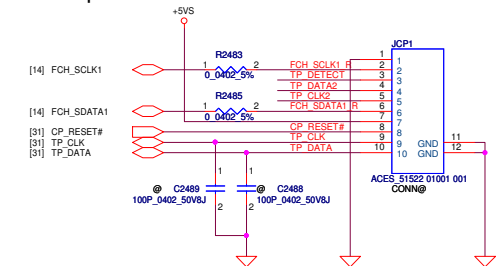
INT\_KBD Conn.



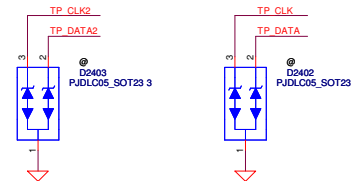
## Track Point Conn



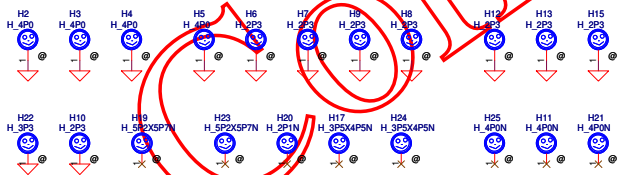
Click pad 10PIN



## ESD Request

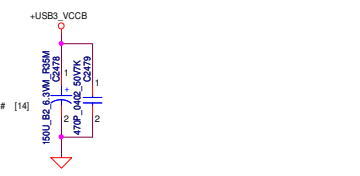
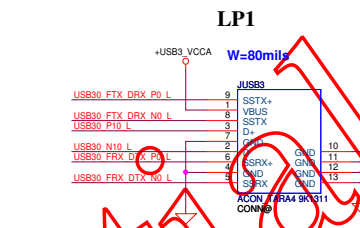
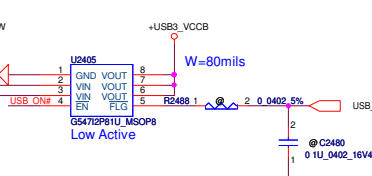
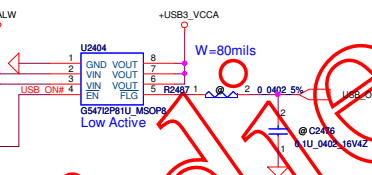
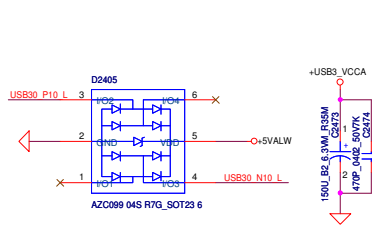
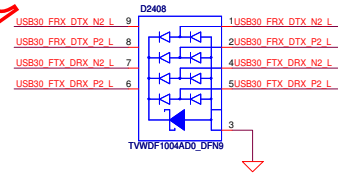
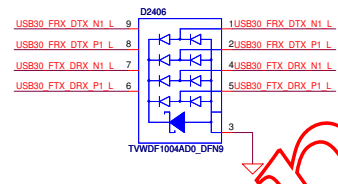
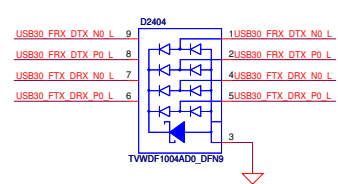
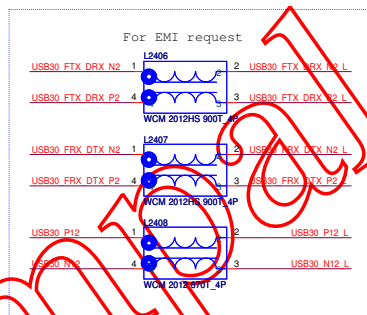
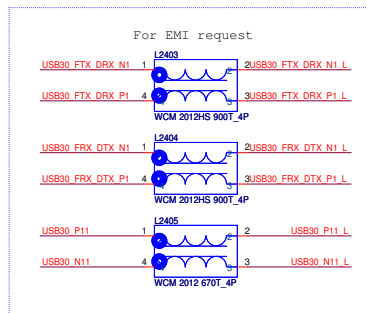
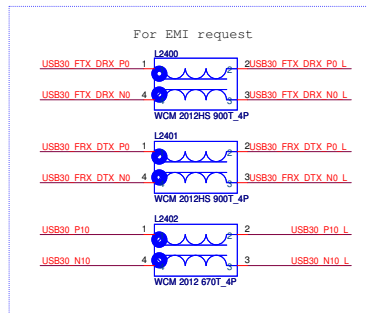
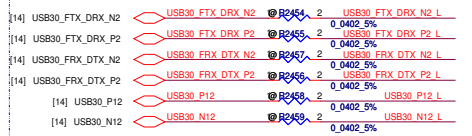
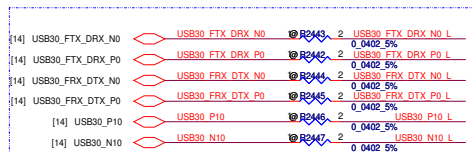


## Screw Holes

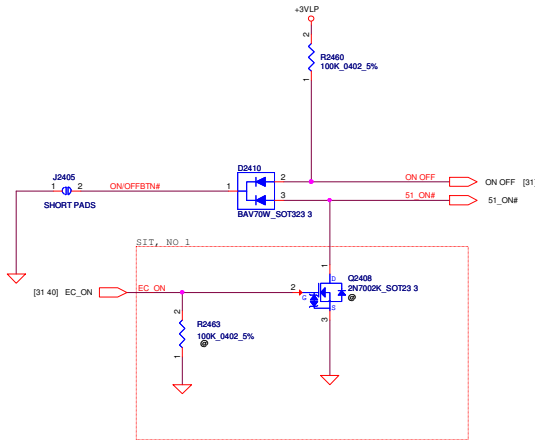


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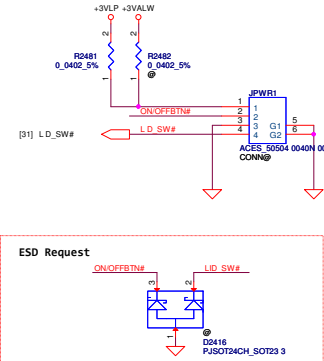
# USB3.0 Conn \*3



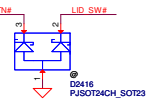
## ON/OFF switch



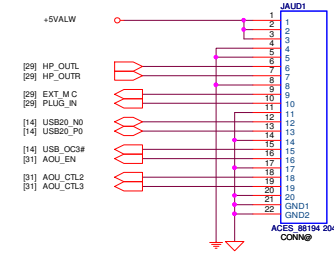
## Power Button Board Conn



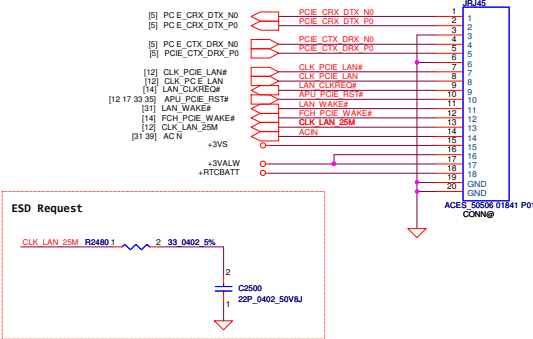
### ESD Request



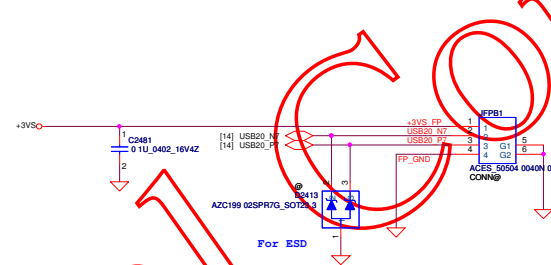
## USB2.0/Audio Jack SB CONN



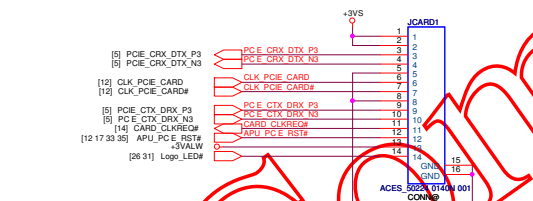
## Lan Conn



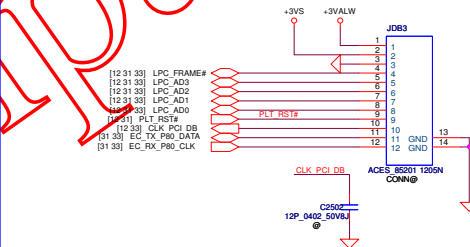
## Finger Printer



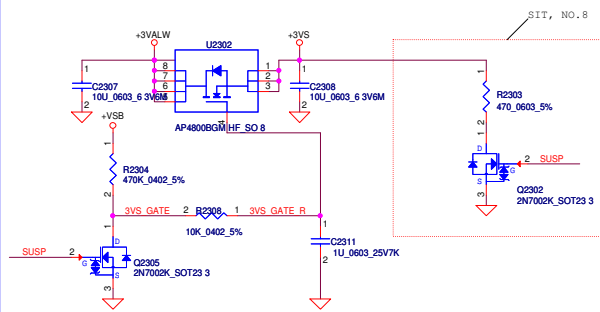
## Card Reader



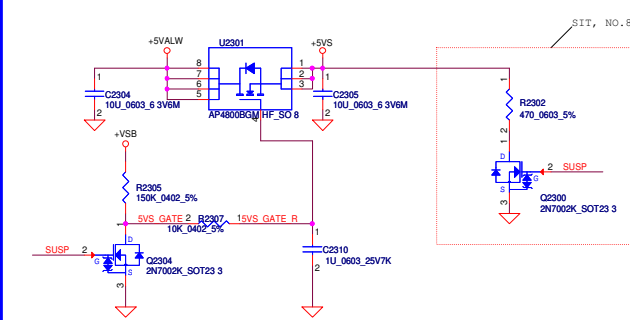
## Debug Conn



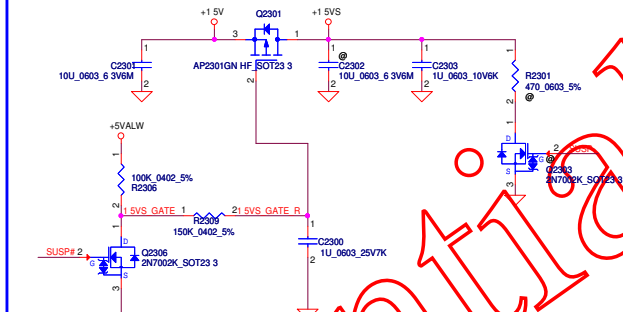
### +3VALW TO +3VS



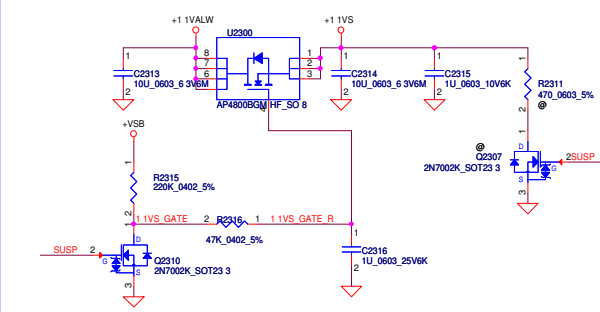
### +5VALW TO +5VS



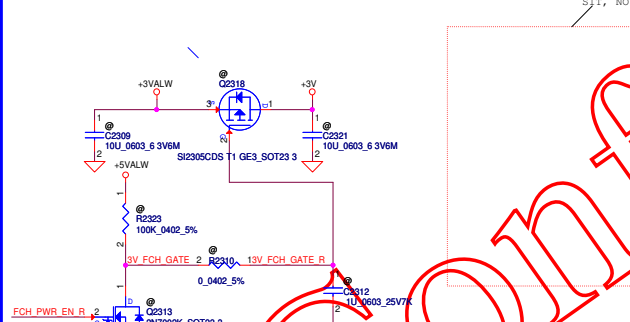
### +1.5V to +1.5VS



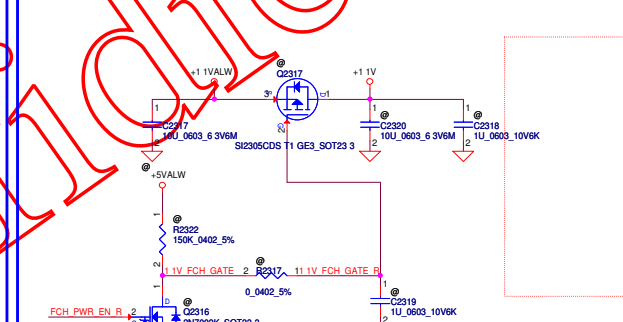
### +1.1VALW to +1.1VS



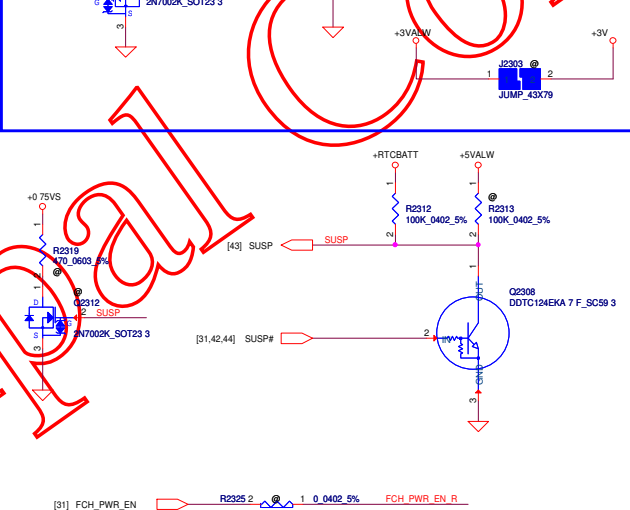
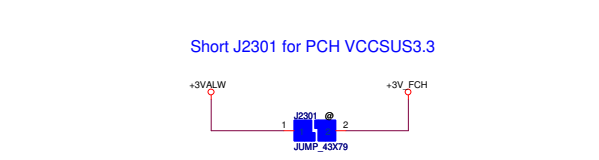
### +3VALW TO +3V



### +1.1VALW to +1.1V

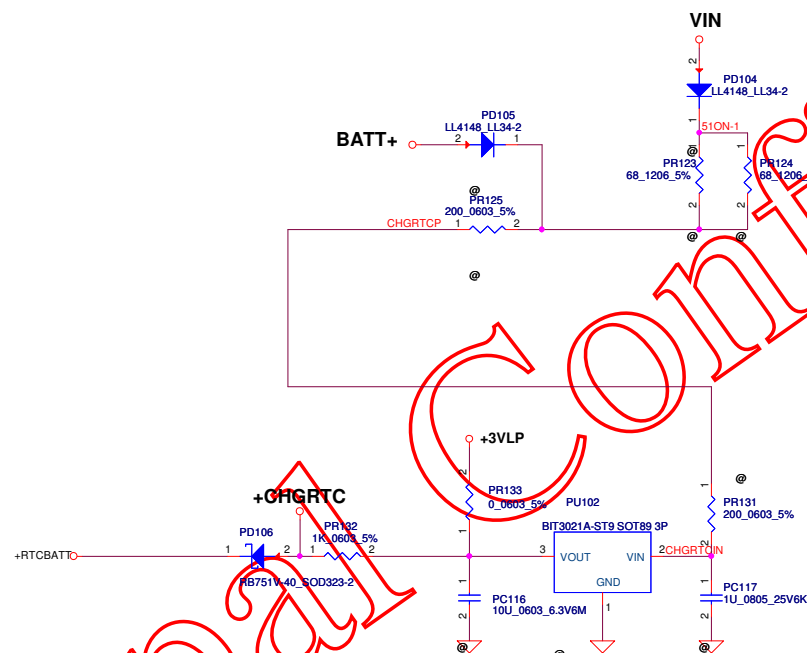
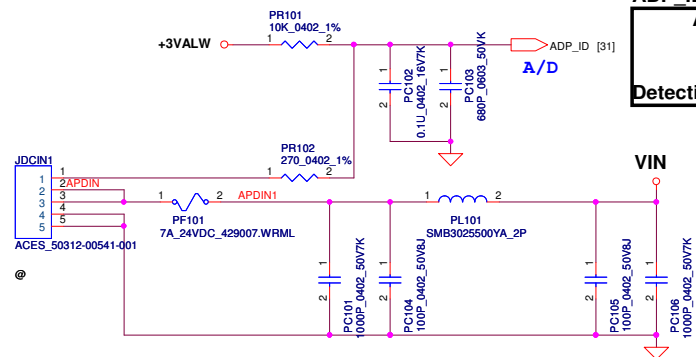


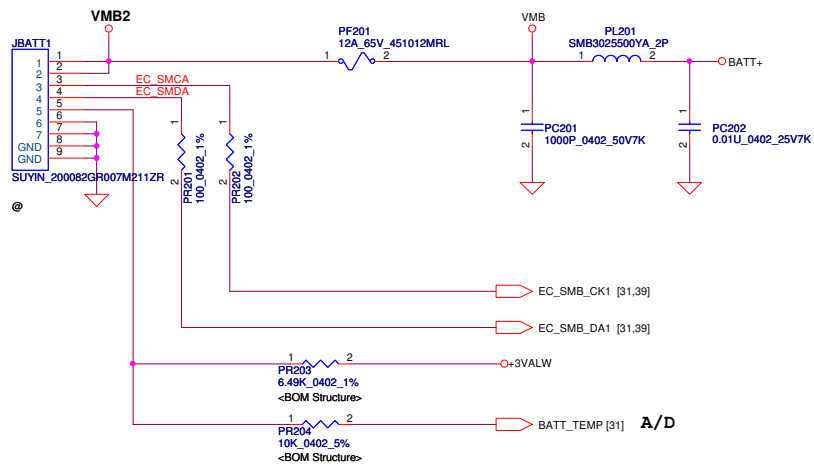
### +3VALW TO +3V\_FCH



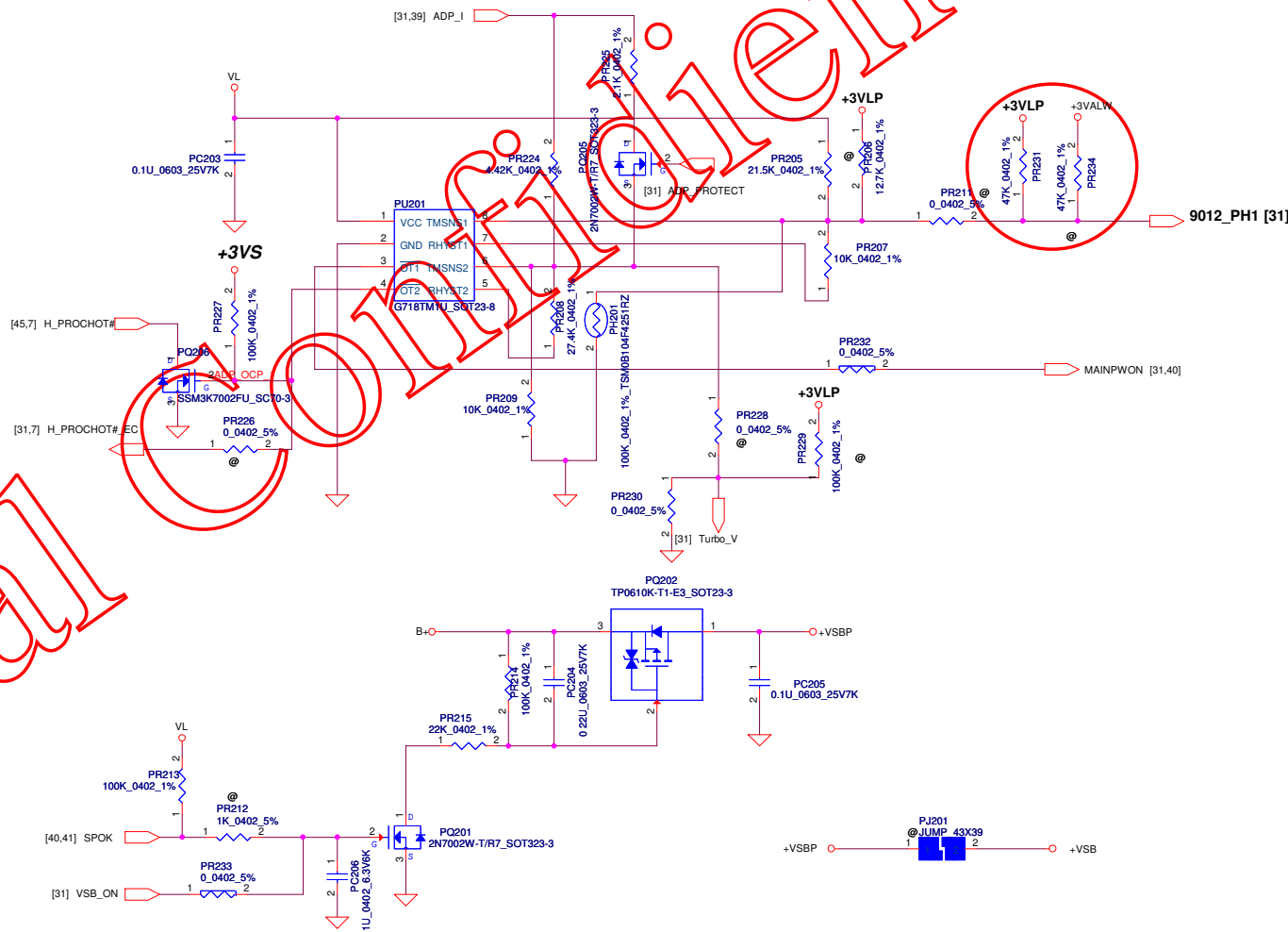
# ADP\_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98

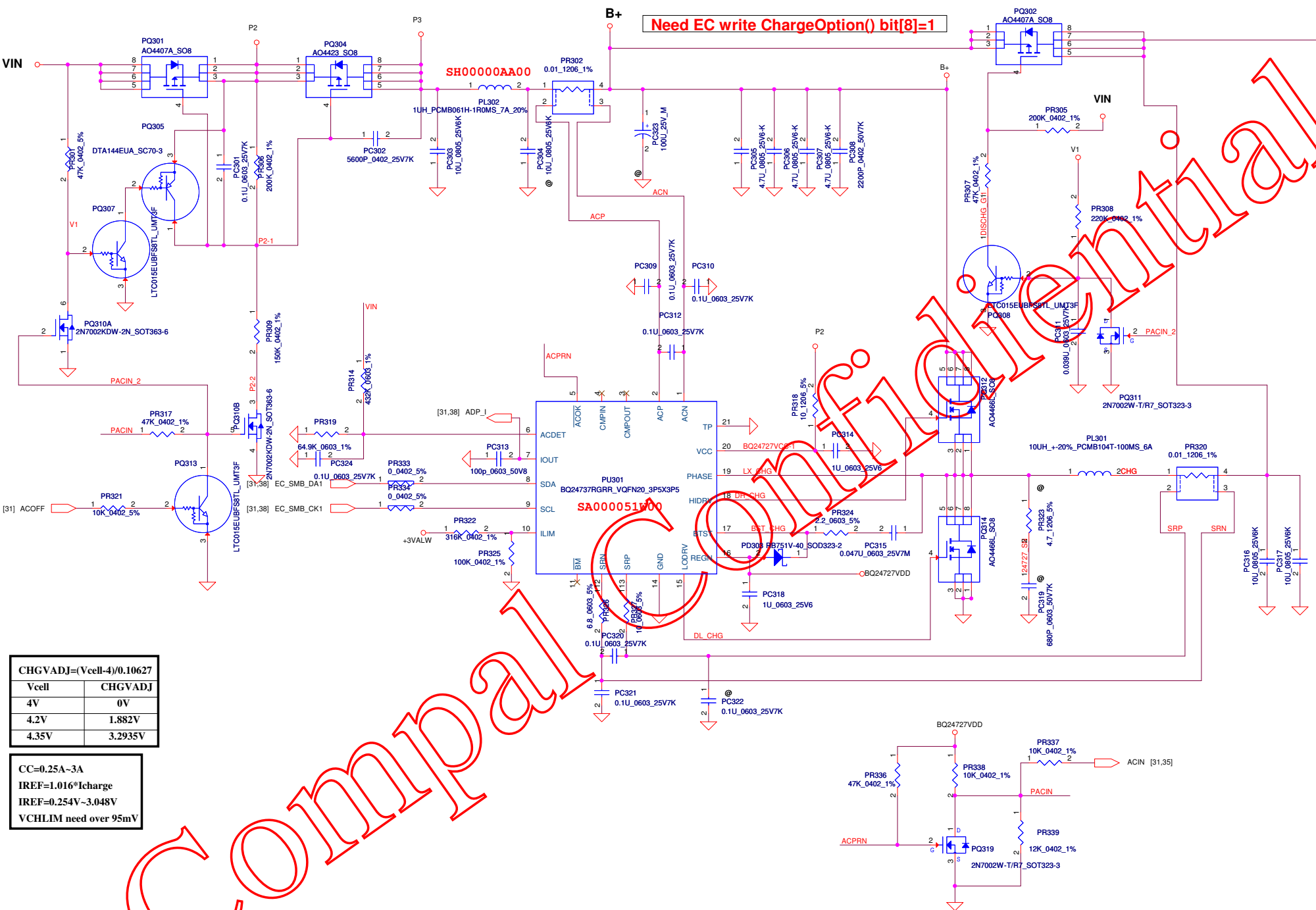




For KB930 --> Keep PU201 circuit  
(Vth = 1.25V)  
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206  
PH201



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CHGVADJ=(Vcell-4)/0.10627

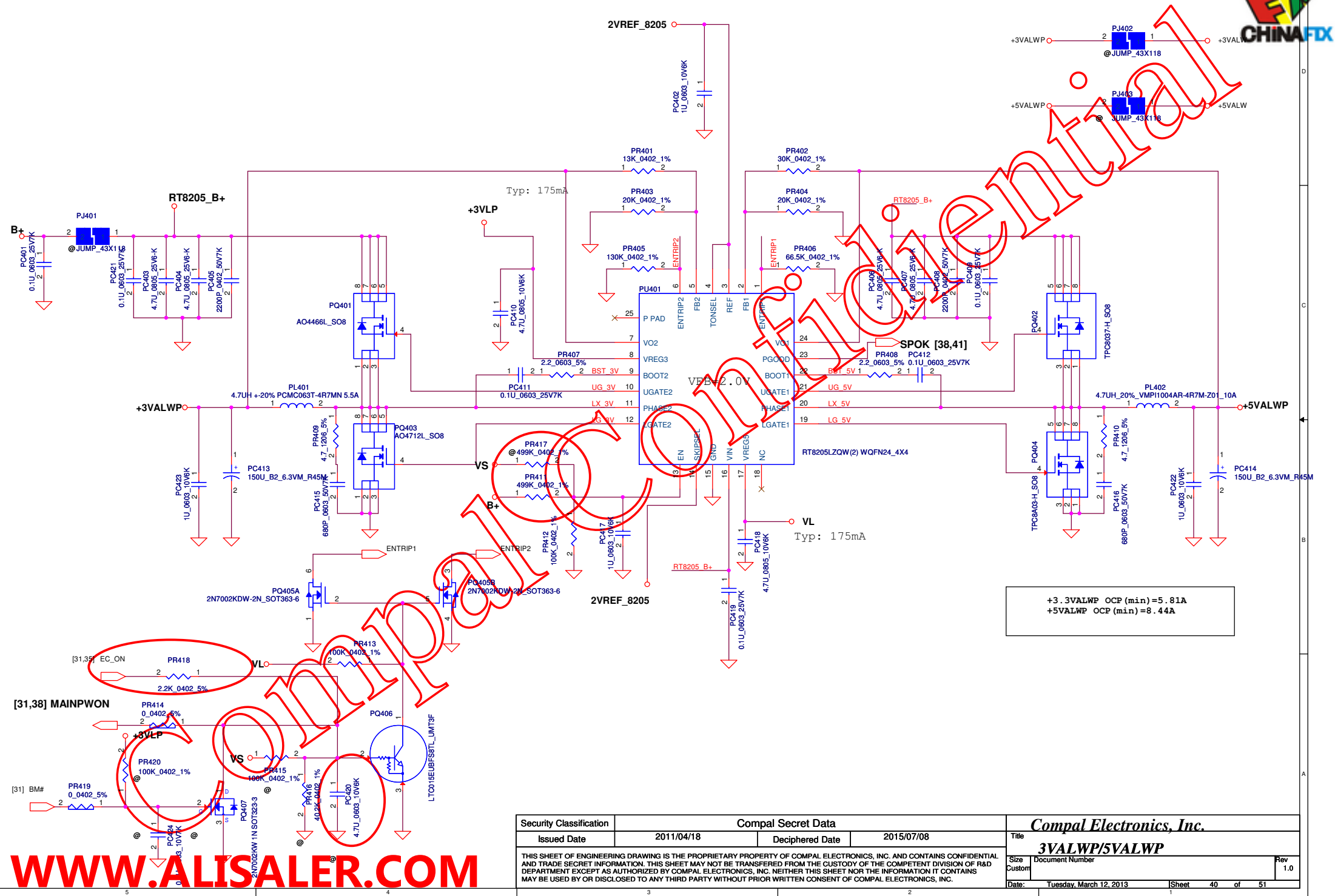
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A  
IREF=1.016\*Icharge  
IREF=0.254V~3.048V  
VCHLIM need over 95mV

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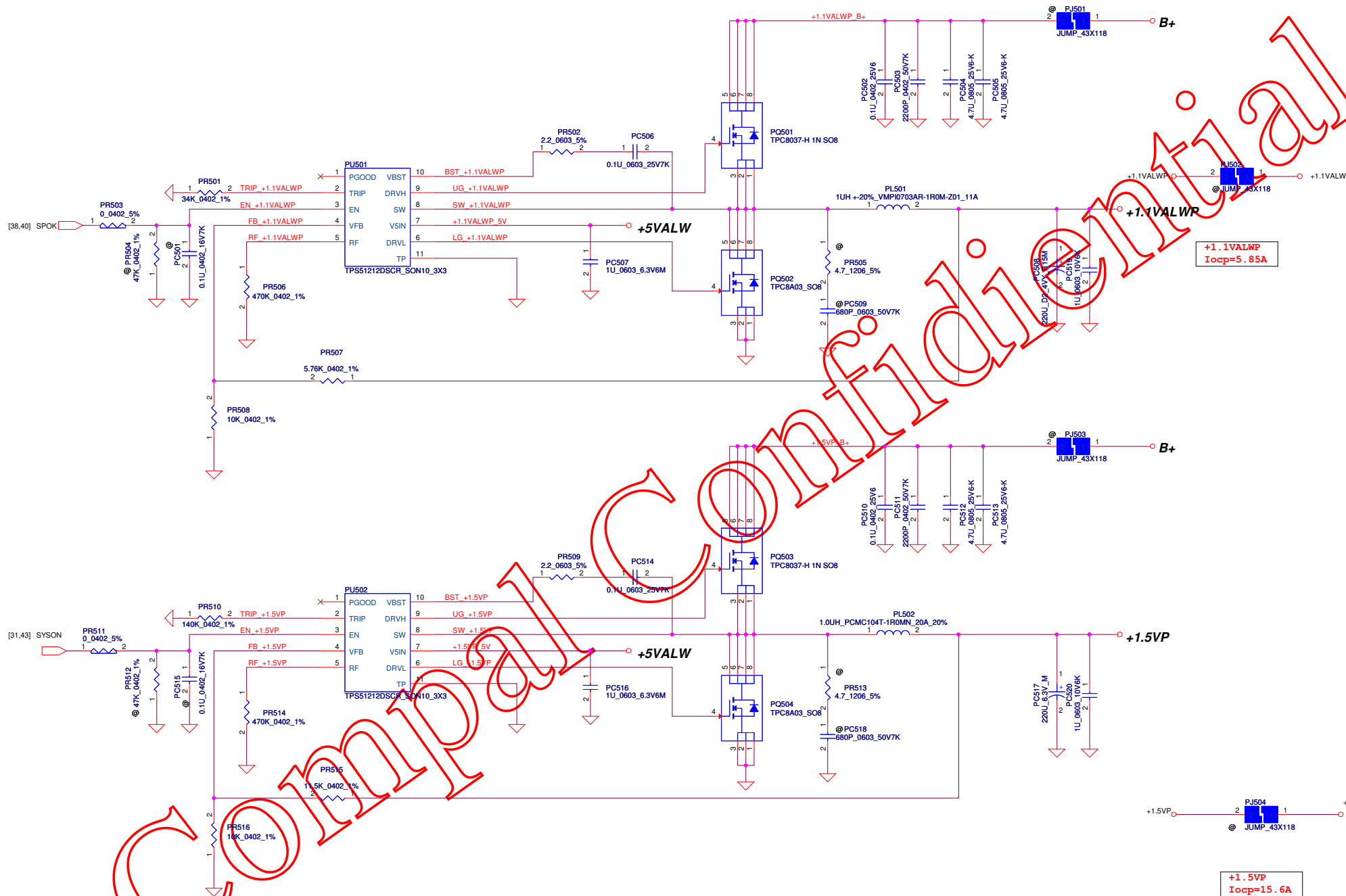
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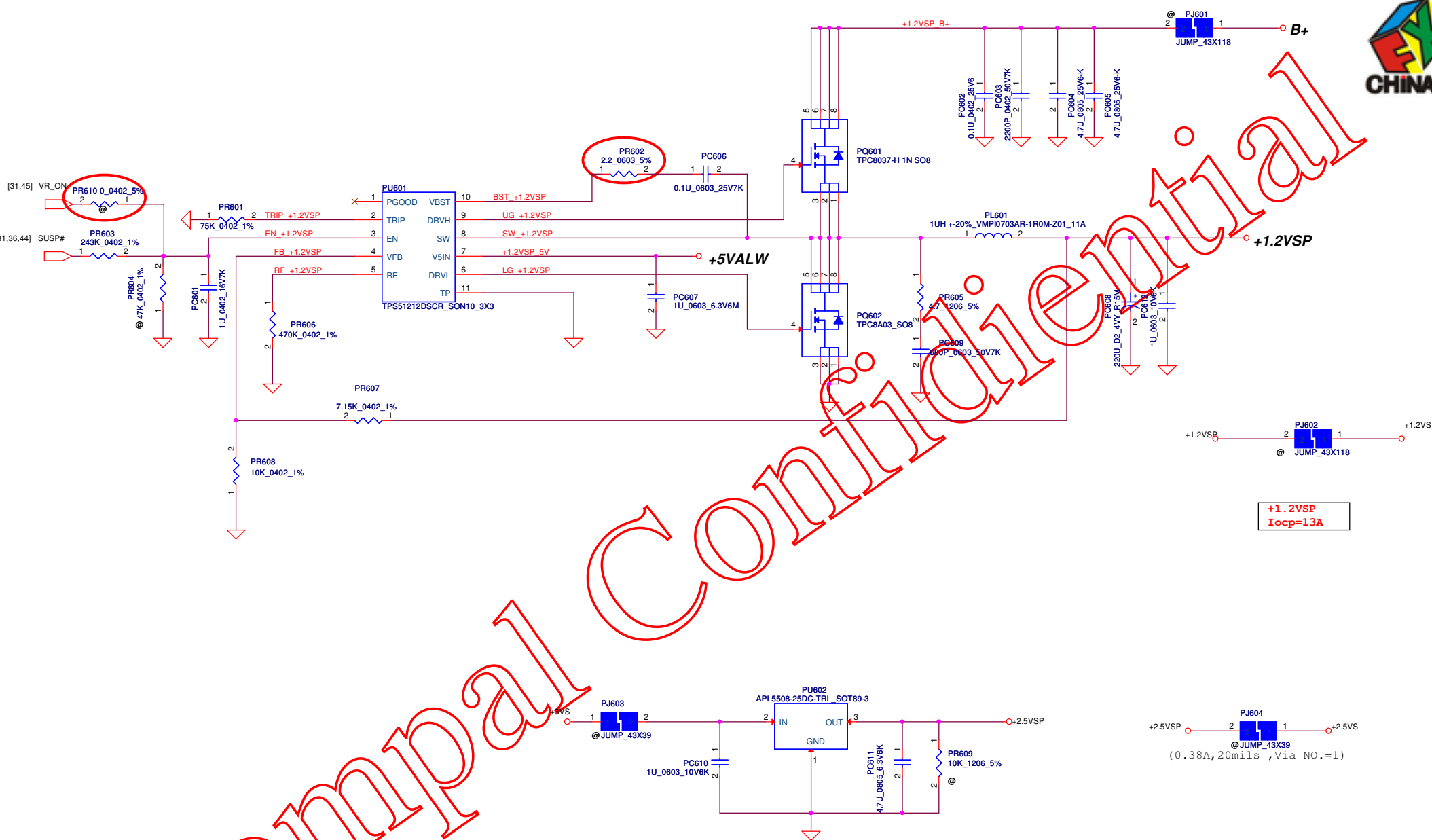
Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO

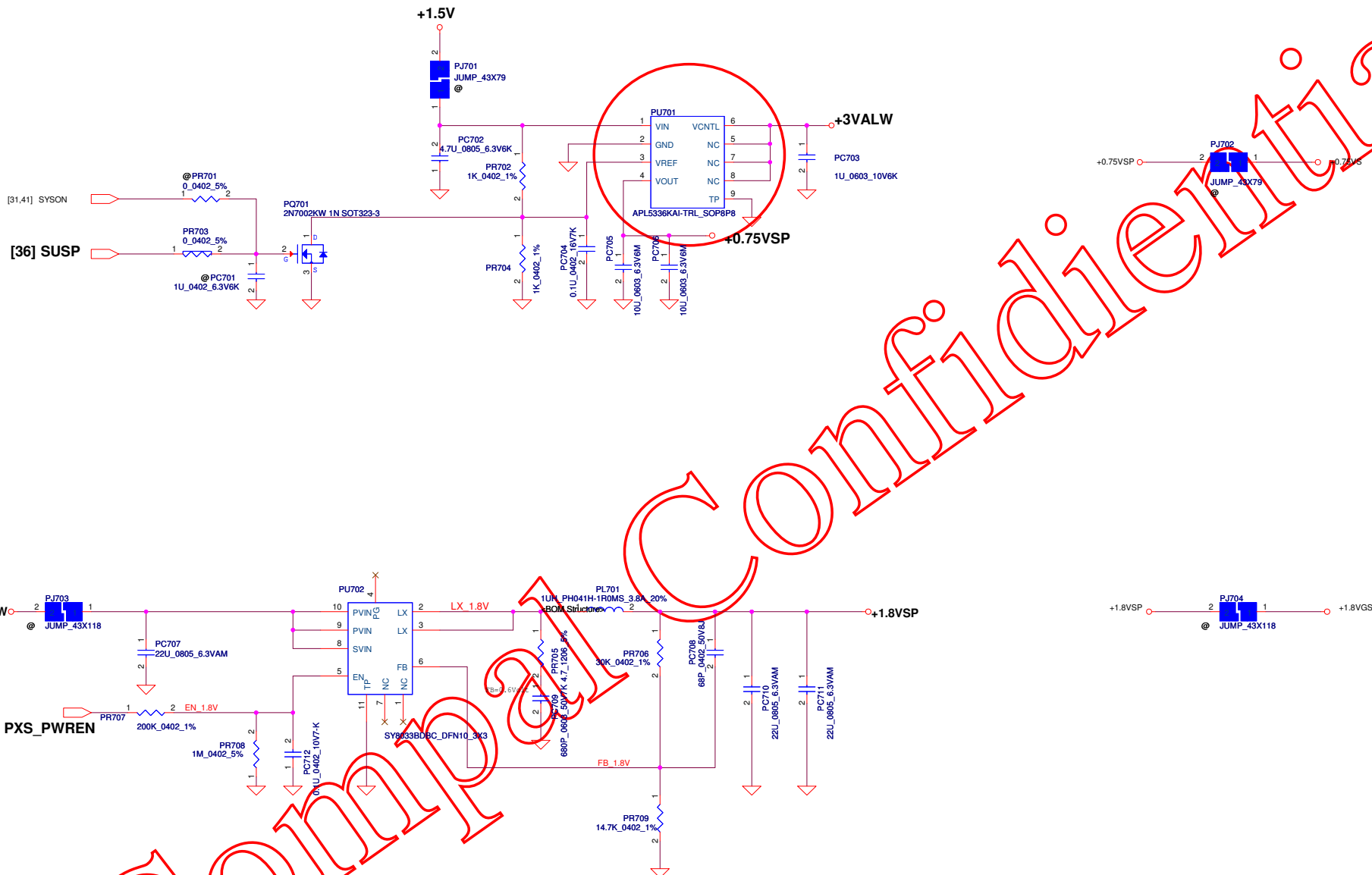


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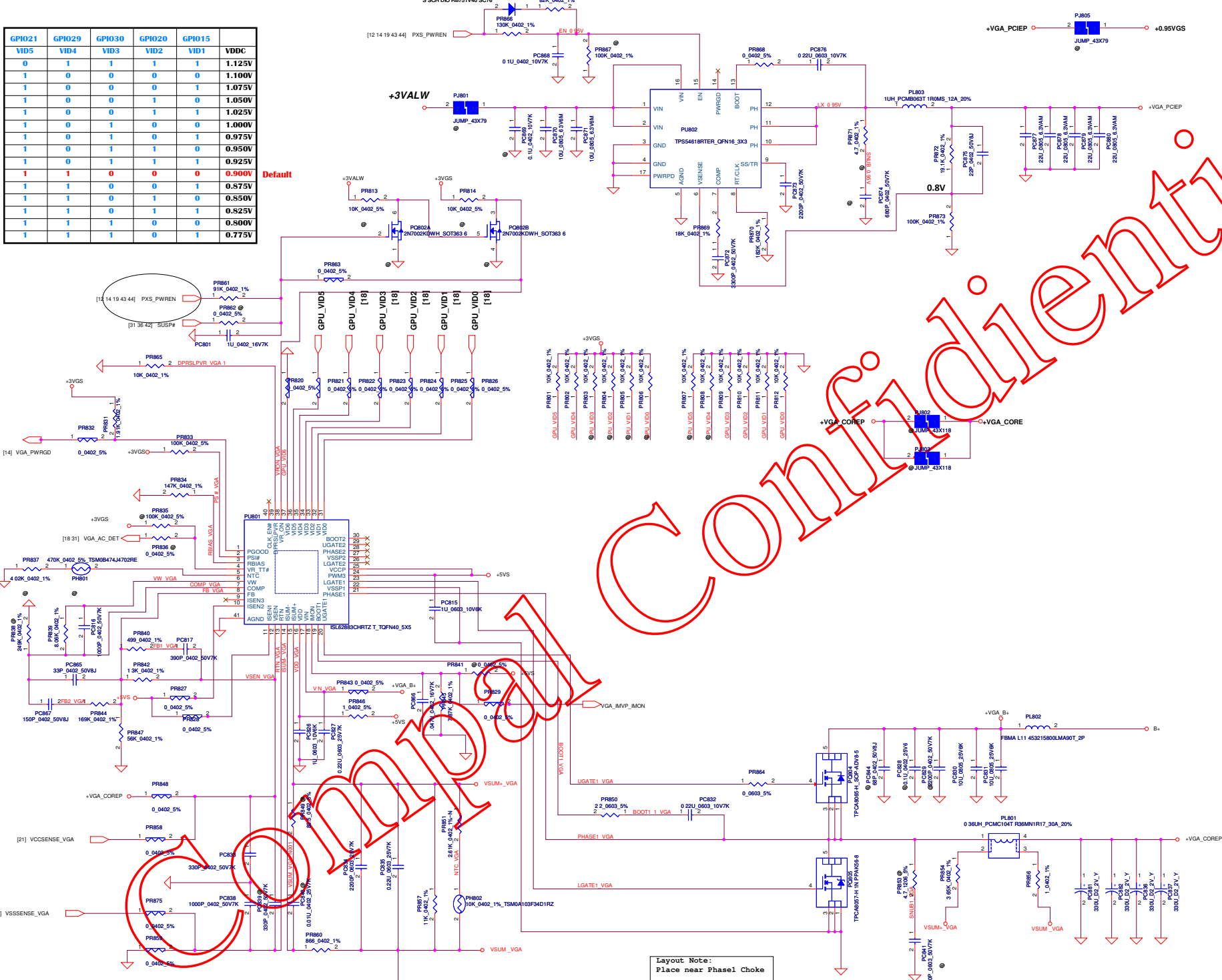




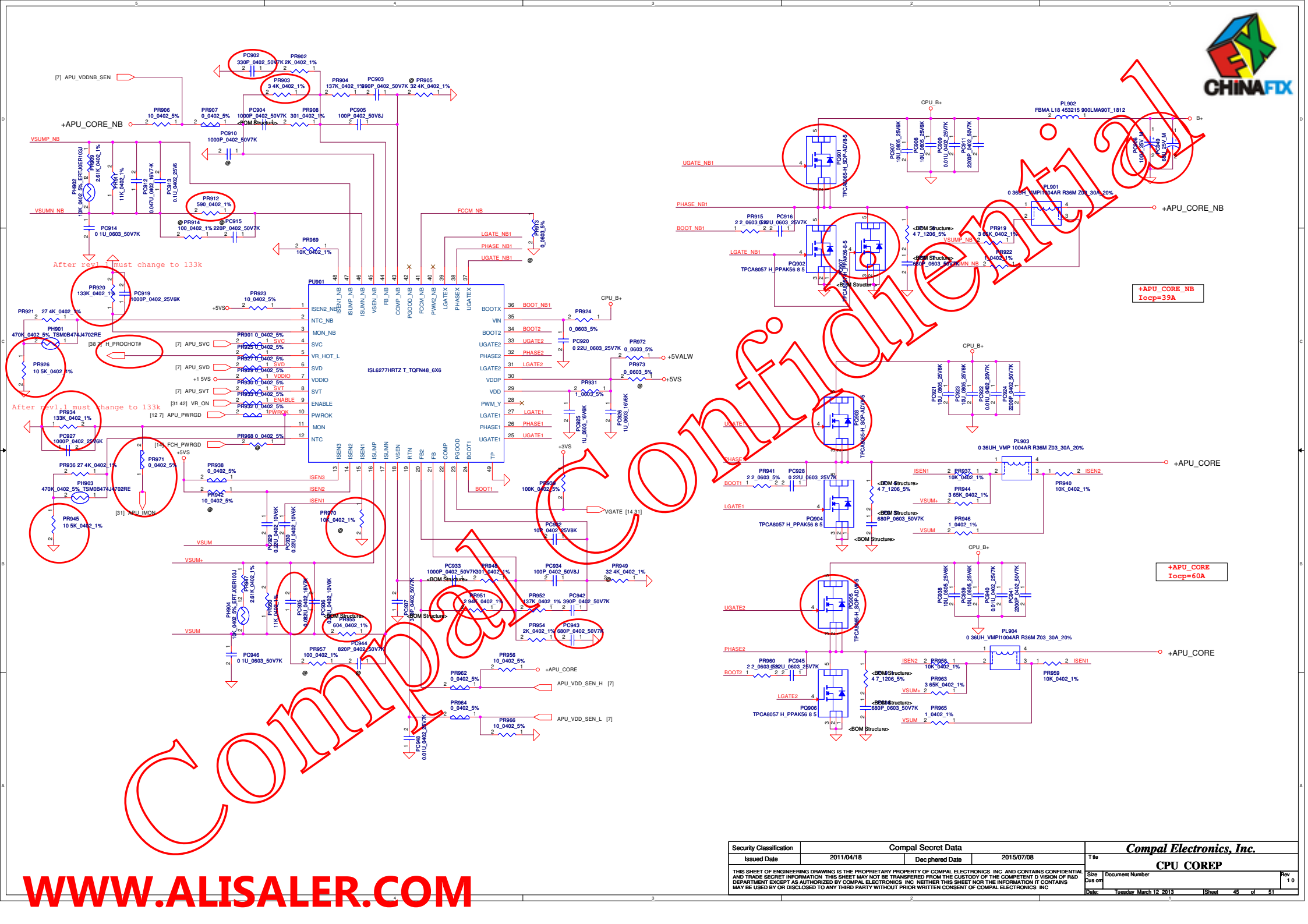


GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	0	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

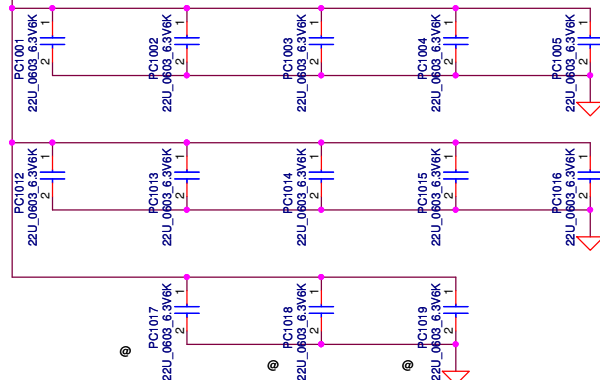
Default



Layout Note:  
Place near Phasel Choke



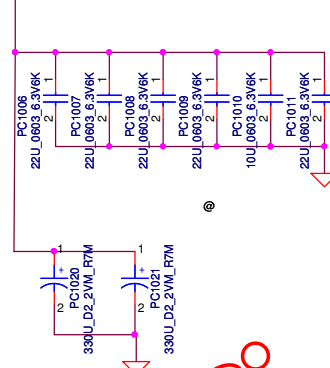
# **+APU\_CORE**



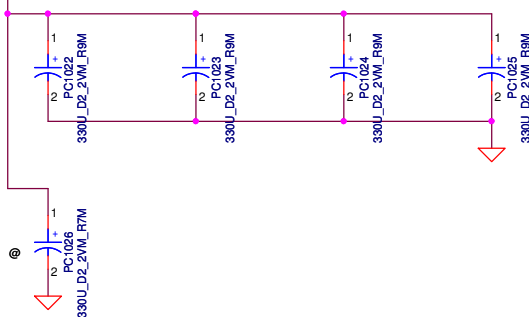
# **+CPU\_CORE**

# **+CPU\_CORE\_NB**

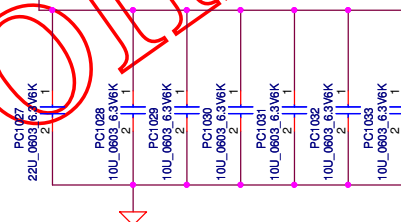
## **+APU\_CORE\_NB**



## **+APU\_CORE**



## **+1.2VS**



## **+1.2VS**

## Version change list (P.I.R. List)

Page 1 of 1  
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107, PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR106, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	Remove PQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
8					
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D

C

B

A

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Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2013/1/10	No.1	v	v	v	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	v	v	v	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	v	v	v	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	v	v	v	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		v	v	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		v	v	Page 32, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	v	v	v	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	v	v	v	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

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